AGH University of Science and Technology
Faculty of Physics and Applied Computer Science

**Doctoral thesis**

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# Front-end electronics in submicron CMOS technologies for tracking detectors in future particle physics experiments

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**Cracow, June 2010**

**Declaration of the author of this dissertation:**

Aware of legal responsibility for making untrue statements I hereby declare that I have written this dissertation myself and all the contents of the dissertation have been obtained by legal means.

**Declaration of the thesis Supervisor:**

This dissertation is ready to be reviewed.

This thesis has been performed in the Department of Particle Interactions and Detection Techniques of the Faculty of Physics and Applied Computer Science, AGH University of Science and Technology in Cracow, Poland and at the European Organization for Nuclear Research (CERN) in Switzerland.

I would like to thank Dr. Jan Kaplon and Dr. Pierre Jarron from the Electronics Systems for Experiments Group at CERN for their support and help during my work at CERN and for valuable scientific discussions.

The author acknowledges support received from the Marie Curie Early Stage Research Training Fellowship of the European Community's Sixth Framework Programme, contract number MEST-CT-2005-020216.

The work performed at CERN in the frame of Marie Curie EST Fellowship was supervised by Dr. Jan Kaplon.

*To my parents,*
*Maria and Kazimierz Półtorak.*

# Streszczenie

Nowe generacje eksperymentów w dziedzinie fizyki wysokich energii pociągają za sobą potrzebę rozwoju nowych technologii, zarówno dla akceleratorów cząstek jak i dla układów detekcyjnych, niezbędnych do precyzyjnego pomiaru produktów zderzeń. Budowa takich eksperymentów jest niezwykle skomplikowanym i kosztownym zadaniem, dlatego projekty oparte na gigantycznych akceleratorach mają charakter globalny i prowadzone są w ramach rozległej współpracy międzynarodowej.

Aktualnie największym na świecie akceleratorem cząstek jest Wielki Zderzacz Hadronów (ang. Large Hadron Collider – LHC) usytuowany w Europejskim Instytucie Badań Jądrowych (ang. European Organization for Nuclear Research — — CERN). Doświadczenie zdobyte podczas przygotowania eksperymentów związanych z akceleratorem LHC i detektorami takimi jak A Toroidal LHC ApparatuS (ATLAS) czy Compact Muon Solenoid (CMS) pokazuje, iż prace badawczo-rozwojowe, zaprojektowanie i przetestowanie wersji prototypowych, produkcja i weryfikacja ostatecznych wersji poszczególnych elementów składowych ogromnych detektorów, zajmuje wiele lat — w przypadku detektorów ATLAS i CMS ponad piętnaście. Z tego względu rozwiązania technologiczne muszą być gotowe w przybliżeniu na pięć lat przed planowanym uruchomieniem eksperymentu.

To doświadczenie jest niezwykle istotne, gdy na horyzoncie pojawiają się nowe generacje eksperymentów fizyki wysokich energii, a mianowicie:

– rozbudowa akceleratora Large Hadron Collider (LHC) do Super-LHC (S-LHC) poprzez zwiększenie jego świetlności,

– budowa liniowego zderzacza elektron-pozyton, którym może być Compact LInear Collider (CLIC) lub International Linear Collider (ILC).

Powyższe przedsięwzięcia mają sens pod warunkiem, że zostaną opracowane odpowiednie technologie detektorowe umożliwiające efektywne wykorzystanie możliwości badawczych oferowanych przez akceleratory. W szczególności, bardzo

ambitne wymagania stawiane są detektorom śladowym, służącym do detekcji torów cząstek naładowanych. Główne wymagania stawiane elektronice do odczytu detektorów śladowych sprawiają, iż układy te muszą być wielokanałowe i zminiaturyzowane, o minimalnym poborze mocy, odporne na promieniowanie oraz zdolne to odbioru i kształtowania sygnałów z detektorów w czasie narzuconym przez częstość zderzeń w akceleratorze. Z tego względu aktualnie prowadzone są prace badawczo-rozwojowe, mające na celu opracowanie prototypowych układów detekcyjnych oraz pokazanie, że spełniają one wymagania eksperymentów planowanych na akceleratorach S-LHC, CLIC i ILC.

W pierwszym rozdziale pracy zostały przedstawione skrótowo projekty nowych akceleratorów, perspektywy nowych eksperymentów, ich znaczenie dla rozwiązania fundamentalnych problemów fizyki cząstek elementarnych oraz wymagania stawiane detektorom do pomiaru torów cząstek w takich eksperymentach.

Główną część prezentowanej pracy doktorskiej stanowią opisy dwóch prototypowych układów elektroniki front-end do odczytu krzemowych detektorów pozycyjnych rozwijanych dla eksperymentów następnej generacji.

Pierwszym z omawianych układów elektronicznych jest układ nazwany ABCN-25. Jest on przeznaczony do odczytu krzemowych detektorów paskowych w detektorze S-ATLAS — rozbudowanej wersji detektora ATLAS, przystosowanej do warunków S-LHC. Wysoka świetlność, duża częstość i energia zderzeń wiązek protonowych oraz duże rozmiary i wysoka granulacja Detektora Wewnętrznego (ang. Inner Detector – ID) w rozbudowanym detektorze S-ATLAS powodują, że elektronika front-end musi być przede wszystkim szybka przy niskim poborze mocy oraz odporna na wysokie dawki promieniowania. Prototypowy układ scalony ABCN-25 został zaprojektowany i wyprodukowany w technologii IBM 0.25 μm. Indywidualny wkład autora w postaci projektów konwerterów cyfrowo-analogowych oraz wewnętrznego układu kalibracyjnego jest opisany szczegółowo w rozdziale drugim. Obwody te mają zapewniać precyzyjne i programowalne poziomy prądów oraz napięć wymaganych do prawidłowego działania i testowania analogowych bloków układu ABCN-25. Architektura tych obwodów została zaprojektowana biorąc pod uwagę przewidywane efekty radiacyjne i związane z tym pogorszenie precyzji układów elektronicznych. Drugi rozdział zawiera wyniki testów prototypowych układów ABCN-25 jak również rezultaty testów radiacyjnych konwerterów cyfrowo-analogowych oraz układu kalibracyjnego.

Drugim z omawianych układów odczytowych jest układ scalony o nazwie roboczej AFRP. Jest on przeznaczony do sprawdzenia nowej technologii detektorów pikselowych,

nazywanej Thin Film on ASIC (TFA), jako potencjalnej opcji dla detektorów wierzchołka przy akceleratorze CLIC. Głównym wymaganiem stawianym detektorom wierzchołka w eksperymentach wykorzystujących zderzenia leptonów jest ich wysoka precyzja. Z tego względu prowadzone są prace badawczo-rozwojowe nad nowymi technologiami detektorów pikselowych zbudowanych z użyciem minimalnej ilości materiału tak, aby zminimalizować wielokrotne rozpraszania badanych cząstek w obszarze detektora. Technologia TFA pozwala na bezpośrednie osadzenie cienkiej warstwy krzemu, rzędu $10 - 30\,\mu m$, na matryce układów odczytowych, zapewniających wysoką segmentację sensora. Trzeci rozdział niniejszej pracy zawiera podsumowanie wkładu autora do projektu obwodów front-end układu scalonego AFRP oraz wyniki testów prototypowego układu scalonego i struktur TFA powstałych przez osadzenie sensora z krzemu amorficznego na prototypowym układzie AFRP.

Zasadniczy tekst niniejszej rozprawy jest uzupełniony trzema dodatkami zawierającymi bardziej szczegółowe informacje dotyczące:

- modelu EKV dla tranzystorów MOSFET,
- modelu szumowego tranzystorów MOSFET,
- analizy szumowej obwodów front-end w układzie scalonym AFRP.

# Contents

# Introduction

Every new generation of High Energy Physics (HEP) experiments requires developing new advanced technologies for the accelerators and for the detectors. Thus, each experiment is preceded by numerous Research and Development (R&D) programs carried out by large international collaborations. Currently, the world's most powerful particle accelerator is the Large Hadron Collider (LHC), located at the European Organization for Nuclear Research (CERN) near Geneva, Switzerland. It is worth noting that R&D projects on new detector concepts and technologies suitable for experiments at the LHC were started at the beginning of nineties of the past century. Then building and commissioning the detectors in big experiments, like A Toroidal LHC ApparatuS (ATLAS) and the Compact Muon Solenoid (CMS), took several years. Therefore, detector technologies and detector designs have to be frozen about five years before the expected start of the experiment.

Keeping in mind experience with designing and constructing detectors for the LHC, the HEP community is already looking at detector requirements for the next generation of experiments, foreseen to start about 2020. There are two big HEP projects being considered for the near future, namely upgrade of the LHC to Super LHC (S-LHC), and a lepton linear collider, which can be either the International Linear Collider (ILC) or the Compact LInear Collider (CLIC). Research potential of these two powerful accelerators can be fully exploited provided one can build adequate detectors. For example, today there are no matured technologies of position sensitive detectors that would meet the requirements of vertex and tracking detectors at the linear collider.

The tracking systems of collider experiments are essential in all physics analysis. The pattern recognition, reconstruction of vertices and measurements of impact parameters of charged particles have to be provided by several layers of high-resolution position sensitive detectors surrounding the collision point. The extrapolated particle path, drawn from back to where it meets with one or more other paths, allows to reconstruct the decay vertices. Identification of secondary vertices, located outside the collision region,

enables a signature for very short-living particles, formed in the collision and then decaying at the secondary vertex location. This information can be applied to discriminate *b*-hadrons, $\tau$ leptons and other short-living particles that characterize rare decay events. Therefore, the precision of particle tracking is of a particular importance for the innermost tracker part — vertex region, where the highest detector granularity has to be provided.

This thesis describes the development of front-end electronics for readout of vertex and tracking detectors in future particle physics experiments. The author has participated in development of two types of readout architectures; one suitable for readout of Silicon Strip Detectors (SSDs) in the ATLAS Inner Detector (ID) Upgrade at S-LHC, and second one for a new type pixel detectors, which potentially can be used at CLIC.

High luminosity and high rate of proton-proton interactions at S-LHC put extreme requirements for fast, low noise, and radiation-tolerant readout electronics for the inner tracker. The concept of the ATLAS Inner Detector Upgrade, and in particular, of the Silicon Strip Detector Tracker (SSDT) is outlined in Chapter 2. Then, the design of the front-end circuitry of the prototype readout chip, called ATLAS Binary Chip Next (ABCN-25), designed and manufactured in IBM 0.25 μm process[1] is overviewed. Specific author's contributions to this development, i.e. the design of radiation resistant Digital-to-Analog Converters (DACs) and of the internal calibration circuitry are discussed in detail. These two circuits are required to provide programmable and precise voltages and currents for the front-end circuit. In order to meet these requirements, taking into account expected radiation effects, new circuit concepts have been developed. The design considerations, evaluation tests and radiation tests for these circuits are presented.

The lepton-lepton collisions as expected at the CLIC put extreme requirements for a high precision vertex detector. The hybrid pixel technology developed and implemented in the current LHC experiments will not meet these requirements, mainly because of too much material being used for the sensors, readout electronics and for services. Therefore, completely new technologies have to be explored to work out suitable solutions. The Thin Film on ASIC[2] (TFA) technology as a possible option for the vertex detector at CLIC is presented in Chapter 3. This is another area with specific author's contribution. The TFA technology is reviewed briefly and then the noise analysis and design of the front-end circuit is discussed in details. The demonstrator ASIC, called Amorphous Frame Readout Pixel (AFRP), composed of an array of 64 by 64 pixelized

[1]The International Business Machines (IBM) Complementary Metal Oxide Semiconductor (CMOS) 6SF process featuring the 0.25 μm lithography, 3 metal levels and power supply voltage of 2.5 V

[2]Application-Specific Integrated Circuit

front-end electronics has been fabricated in IBM 0.25 μm process. The test results of final TFA structures, containing 10 μm thick sensor samples deposited on a demonstrator chip, are reported and discussed.

The thesis is complemented by three appendixes including more detail information on: the Enz-Krummenacher-Vittoz (EKV) model used for noise optimization of the front-end circuits (A), noise models of Metal-Oxide Semiconductor Field-Effect Transistor — MOSFET (B) and detailed noise analysis of the TFA front-end circuit (C).

# Chapter 1

# Future high energy physics accelerators and experiments

## 1.1 Present state of high energy experimental physics

Physics theories and discoveries carried out over the past century have resulted in significant insight into the common and well established picture of the subatomic world, called the Standard Model (SM) of particle physics. This model provides an explanation of fundamental interactions: electromagnetic, weak and strong forces, as well as a description of elementary particles, which make up all observable matter in the universe. The SM was developed in the early 1970's, and since then, it has become a well-tested physics model, thanks to the outcome of a large variety of high energy physics experiments. The complex experimental verifications of the SM were carried out through a synergy of several types of particle colliders: hadron-hadron (e.g. Tevatron), lepton-hadron (Hadron Elektron Ring Anlage — HERA) and lepton-lepton (e.g. Large Electron Positron Collider — LEP). Since one part of the SM, concerning the origin of particle mass, has yet to be proven in any experiment, the race to hunt for the potential exhibit — the Higgs boson — is on. Furthermore, the SM does not include a description of gravitional interactions, nor does it give an answer for important questions, such as, what is the nature of dark matter and dark energy, what happened to the missing antimatter, and more. In order to find the missing pieces of the puzzle, new information from the experiments is indispensable.

Currently, the world's most powerful particle accelerator is the Large Hadron Collider (LHC). The machine is located at the European Organization for Nuclear Research near Geneva, Switzerland. The LHC is designed to collide two circulating beams of protons or

heavy ions in a 27-kilometer ring, buried around 50 to 175 meters underground. The final conceptual design report [1] describes a challenging machine, optimized for a nominal luminosity of $1 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ at 7 TeV proton beam energy. The beams move around the LHC ring inside a continuous vacuum, guided by superconducting magnets with a field of 8.4 T. The magnets are cooled by an enormous cryogenic system filled with superfluid helium kept at a temperature of 1.9 K. The collisions take place inside the four main LHC experiments: ATLAS, CMS, A Large Ion Collider Experiment (ALICE) and the Large Hadron Collider beauty (LHCb). The LHC is designed to provide a rich program of physics at a new high-energy frontier over the coming years. Above all, it should confirm or refute the existence of the Higgs boson, the last missing piece of the Standard Model. The LHC will also explore the possibilities for physics beyond the SM, such as supersymmetry, extra dimensions and new gauge bosons. The discovery potential is huge [2] and the results will set the direction for possible future high-energy colliders. Nevertheless, scientists have already made some steps towards the post-LHC era. In order to extend the physics reach of the LHC experiments, more statistics of interesting events will be needed. In parallel, a better understanding of possible new LHC discoveries, together with the detailed knowledge of any new particles, will be essential for comprehending physics behind the SM.

There are two distinct and complementary strategies for the next steps towards future HEP experiments:

1. High energy approach providing direct discovery potential for new phenomena by colliding particles at very high energies. This is achieved in hadron colliders which can provide required center-of-mass energy. The price to pay are variations in collision energy due to the fact that hadrons are composite particles, and high background from strong interactions.

2. High precision approach probing new physics at high energies through precision measurements of phenomena at lower energy scales. This approach is based on lepton collisions at a tunable but limited beam energy. The benefit of this approach is the well known collision energy of point-like leptons and a moderate amount of background.

The future HEP experiments follows both complementary approaches. This leads to, firstly, an upgrade of the LHC machine together with its experiments (high energy approach) and secondly, the electron-positron colliders, which provide research complementary to the LHC (high precision approach). In this chapter, both approaches are

reviewed briefly, namely the LHC Upgrade called Super-LHC and the CLIC, as the examples of hadron-hadron and lepton-lepton colliders, respectively.

## 1.2 Future hadron collider: Super-LHC

The studies of the LHC upgrade, aiming at an increase of the luminosity from the nominal value of $10^{34}\text{cm}^{-2}\text{s}^{-1}$ up to $10^{35}\text{cm}^{-2}\text{s}^{-1}$ have started in 2001. The first feasibility study [3] has considered several initial upgrade scenarios, including doubling each proton beam energy up to 14 TeV [4]. An investigation of the LHC upgrade focuses on two main subjects: achievable physics potential and implications for the accelerator. From this point of view, doubling the center-of-mass energy would require replacing more than 1000 superconducting dipoles in the accelerator tunnel with stronger magnets [5], which would impose very high costs and involve technical challenges. Therefore, only the scenarios of luminosity upgrade are considered presently and are discussed in this thesis. They are based on an upgrade of the LHC machine and the CERN proton injectors, foreseen to be performed in two phases, as follows [6]:

– *S-LHC Phase I* will aim to achieve a luminosity of $2\text{–}3\times10^{34}$ $\text{cm}^{-2}\text{s}^{-1}$ by an LHC Interaction Region (IR) upgrade, through the replacement of IR magnets, with minimal impact on the experiments. In parallel, the proton beam will be accelerated through the LINAC4, currently under construction, in order to provide higher beam intensity.

– *S-LHC Phase II* will aim to reach an ultimate luminosity of $10^{35}$ $\text{cm}^{-2}\text{s}^{-1}$. This phase foresees further improvements in the injector chain, namely two new injector-accelerators, the Superconducting Proton Linac (SPL) and the Proton Synchrotron 2 (PS2), will replace the Proton Synchrotron Booster and the Proton Synchrotron, respectively. Furthermore, the major upgrades of the ATLAS and CMS detectors are foreseen, and, possibly, another upgrade of the interaction regions. Several scenarios of this phase are being investigated. All of them aim at an integrated luminosity of $3000\,\text{fb}^{-1}$ per experiment, in comparison to about $700\,\text{fb}^{-1}$ integrated luminosity projected before starting the *S-LHC Phase II* [7]. However, the considered scenarios show different approaches to this goal, such as [8]:

  – improved beam focusing, which would require positioning of the IR magnets deep inside the experiments,

– increasing the beam currents, which would be more demanding for the machine in terms of beam dynamics, machine-protection, radiation protection and beam injection, however the beam magnets would not be needed to be placed inside the experiments.

### 1.2.1 Prospects for physics.

A conclusive judgement of what will be the most interesting topics to study in the S-LHC can not be set at this stage and will be established only after a few years of LHC operation at the nominal luminosity. Nevertheless, one can not freeze the study and preparation for future experiments, while waiting for answers to be given by the LHC. We shall assume that the LHC physics program [2] will have been accomplished. An increase by up to one order of magnitude in the integrated luminosity should extend the LHC discovery reach by about 20–30% in terms of the mass of new objects, and allow additional and more precise measurements to be performed [5]. The enhanced discovery potential has been widely studied in Refs. [4] and [9]. According to these papers, the S-LHC goals can be roughly divided into the following main topics:

1. Improvement of the accuracy in determination of Standard Model parameters (e.g. Higgs couplings).

2. Improvement of the accuracy in determination of new physics parameters possibly discovered at the LHC (e.g. s-particle spectroscopy).

3. Extension of the discovery reach in the high-mass region (e.g. quark compositeness, new heavy gauge bosons, multi-TeV squarks and gluinos, extra-dimensions).

4. Extension of the sensitivity to rare processes (e.g. Higgs-pair production, multi gauge boson production).

### 1.2.2 Overview of the detector system.

The main advantage of the S-LHC program is to extend the understanding of fundamental interactions and possible new LHC discoveries, at a moderate additional cost, relative to the overall initial LHC investment. In order to fully profit from the luminosity upgrade, the detector systems in the ATLAS and CMS experiments should present performance similar to the LHC case but at higher particle fluxes in the detectors. An issue appears for the trackers, which should demonstrate good tracking capabilities

in an environment with a much higher particles flux. For the calorimeters, the challenge is to maintain good reconstruction capabilities, through more sophisticated and focused analysis strategies. The foreseen high particle and background rates and the integrated radiation doses do not require replacement of the magnets and most of the calorimeters as well as the muon chambers in the ATLAS experiment. Nevertheless, the inner trackers, forward detectors and a significant part of the readout electronics will need to be redesigned and completely replaced [9]. The current ATLAS Inner Detector consists of a silicon pixel detector as the innermost part, a SemiConductor Tracker (SCT) based on silicon strip detectors and a Transition Radiation Tracker (TRT) in its outer part [10] . The ATLAS ID was designed for an integrated luminosity of up to approximately 700 $fb^{-1}$, thus it would reach the end of its lifetime due to radiation damage at the beginning of the *S-LHC Phase II*. Furthermore, the detectors in S-LHC environment will face radiation damage 4 to 5 times higher than in the LHC case [11]. Thus, the sensors and the front-end electronics employed in the upgraded ID need to be sufficiently radiation tolerant. Current planar silicon sensor technology is suitable for detectors in the ID at a radii higher than 10 cm, where the fluence will be less than $10^{15}\,1-\mathrm{MeV}$ neutron equivalents per $cm^2$ ($n_{eq}cm^{-2}$). However, the innermost part of tracker is expected to face fluence up to $2\times10^{16}$ $n_{eq}cm^{-2}$ at a radius of 3.7 cm, requiring an entire new sensor technology or replacement every few years [11] in case of using present sensor technology.

Not only radiation tolerance will be an issue for the upgraded ID, but also the detectors occupancies. The expected number of proton-proton interactions per beam crossing (pile-up events) is foreseen to 300–400, what gives an increase by a factor of 15 to 20 in comparison to the LHC [11]. In the new environment, the present innermost strip layers of ATLAS SCT, at a radius of around 25 cm, would have occupancies above 10%, whereas the TRT would face occupancy approaching 100%. Therefore, a greater tracker granularity will be provided by silicon pixels in the inner part, at the radius less than approximately 30 cm, and the SSD in the outer part, with a radius up to about 100 cm [11]. Furthermore, it is assumed that strips of different lengths will be used in the middle and outer layers in order to keep the strip occupancy and detector leakage current at acceptable levels. The maximum strip occupancy for SSD should be kept below 2% to guarantee robust pattern recognition. The proposed layout of the upgraded ATLAS Inner Detector, driven by an expected fluence distribution in the tracker, as shown in Fig. 1.1.

At a radius of 5 cm, the fluence is about $10^{16}n_{eq}cm^{-2}$, at 30 cm it decreases to about $10^{15}n_{eq}cm^{-2}$ and at 70 cm it is about $4\times10^{14}n_{eq}cm^{-2}$. This outlines three separate

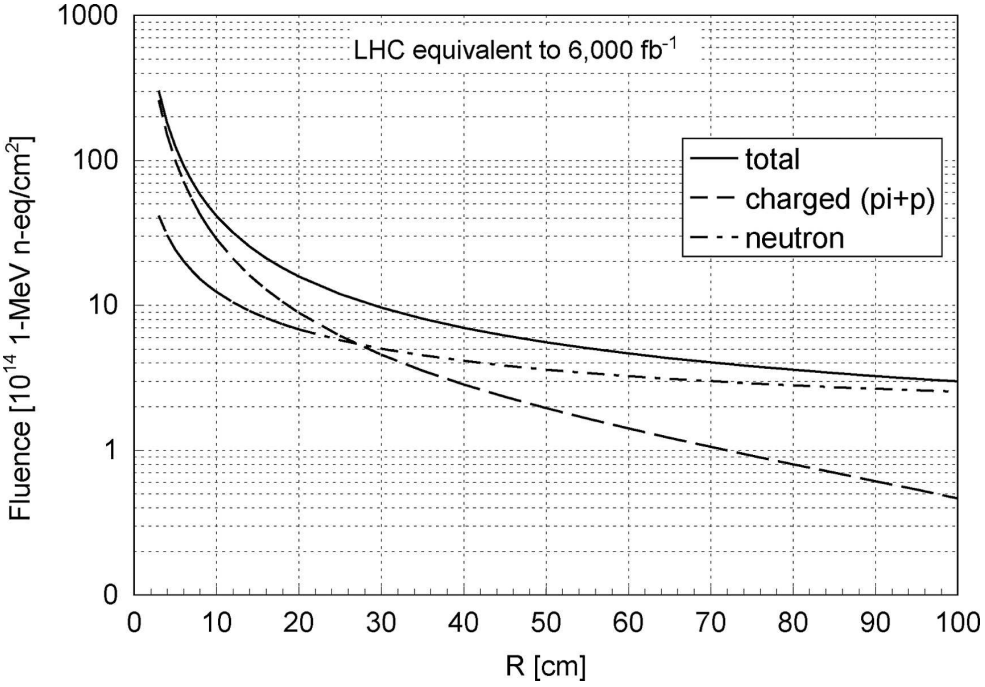



**Figure 1.1:** Particle fluences expected in the Inner Detector of the ATLAS detector at SLHC for an integrated luminosity of 6000 $fb^{-1}$, i.e., the nominal luminosity of 3000 $fb^{-1}$ with a safety factor of 2 [11].

radial regions in the tracker volume, where three different detector layouts should be applied [12], namely:

- **4 Pixel Layers** at radius 5 cm, 9 cm, 18 cm and 27 cm made of silicon pixel type detectors. Most likely, new approaches and concepts for pixel technology are required.
- **3 Short Strip Layers** at radius 38 cm, 49 cm and 60 cm composed of 2.4 cm long silicon strip detectors.
- **2 Long Strip Layers** at radius 75 cm and 95 cm composed of 9.6 cm long silicon strip detectors.

The most recent layout of the upgraded ID is presented in Fig. 1.2.

The crucial issue for the ATLAS Inner Detector Upgrade is the development of the detectors, the front-end electronics and the optoelectronic readout, which will be able to survive under the S-LHC radiation conditions. In addition, the upgraded ID must provide sufficient detector efficiency and readout speed at high incoming data rates. The particular case of the SSD and its readout electronics is briefly described further in Section 1.4.1 of this chapter.

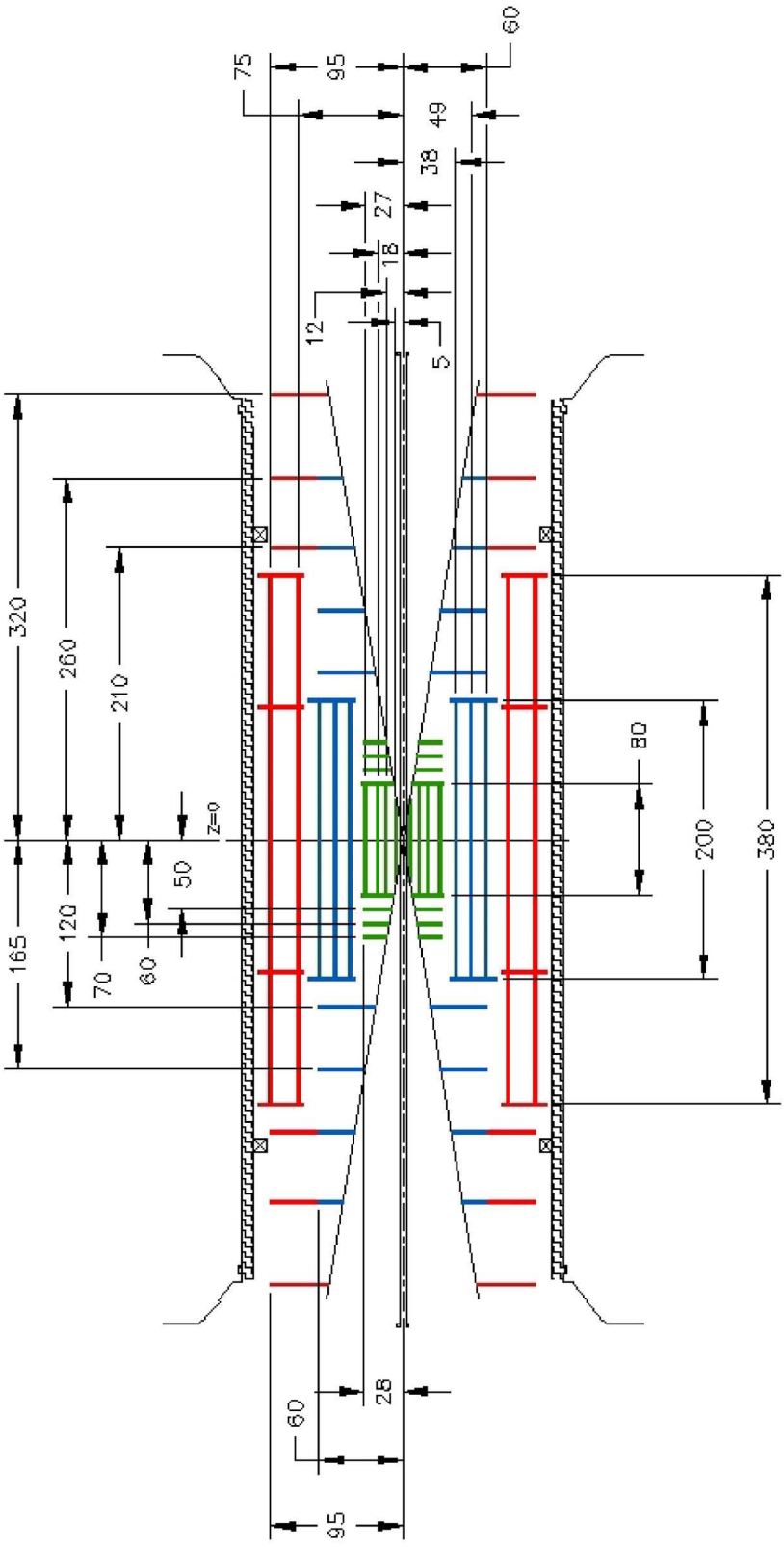



**Figure 1.2:** Proposed layout of the upgraded ATLAS Inner Detector: the pixel layers (green), the short strips (blue) and the long strips (red) [13].

## 1.3 Future lepton colliders: the Compact Linear Collider and the International Linear Collider.

Other possible future HEP experiments for the post-LHC era are based on lepton linear colliders. Currently, there are two major proposals for linear colliders, namely the Compact Linear Collider driven by CERN, and the International Linear Collider driven by Global Design Effort (GDE), for which no decision for the location has been made yet. The main advantage of electron-positron collisions, in comparison to the hadron ones, is the well-defined initial energy of physics events equal to the center-of-mass energy due to point-like electron-positron collisions [14]. In addition, the background of low energy events is negligible in comparison to hadron collisions. CLIC is a challenging project that proposes colliding beams of electrons and positrons at a center-of-mass energy of 500 GeV, which is intended to be later upgraded to 3 TeV. The nominal luminosity goal is in a range of $10^{34} - 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ [15]. In order to reach this energy in a realistic and cost efficient way, very high accelerating gradient has to be applied. According to Ref. [16], the acceleration field in CLIC is aimed at $150\,\mathrm{MVm}^{-1}$, which is outside the reach of available superconducting technology and can only be achieved by a room temperature wave structure travelling at high frequencies of 30 GHz. An interesting feature of this project is a novel concept of the Two-Beam Acceleration (TBA) technique, where the Radio Frequency (RF) power for the main linac sectors is extracted from a secondary, low-energy, high-intensity electron beam running parallel to the main linac. A 150 A intense drive beam, while decelerating from 2 GeV to 200 MeV, produces a power of 230 MW. This power is extracted from the "driving" beam by special Power Extraction and Transfer Structures (PETS) and transferred to the 1 A intense main beam, which is then accelerated from 9 GeV to 1.5 TeV at a gradient of $150\,\mathrm{MVm}^{-1}$. It is planned that a single "driving" beam will provide the main beam acceleration of about 70 GeV, meaning about 22 "drive" beams will be needed in order to achieve 3 TeV main beam energy. This concept leads to a quite simple tunnel, which doesn't contain any active RF components (klistrons). The CLIC accelerator would cover a total length of up to 50 km [15]. Two interaction points are foreseen, one for $e^+$-$e^-$ and one for $\gamma$-$\gamma$, as shown in Fig. 1.3. CLIC may be used also as a photon collider based on the Compton scattering of laser light on the high energy electrons beams [17].

In parallel to the on-going CLIC R&D program, the Global Design Effort is continued on the International Linear Collider design. The 30 km long so-called "cold machine" is based on superconducting cavities, where the electrons and positrons will be accelerated

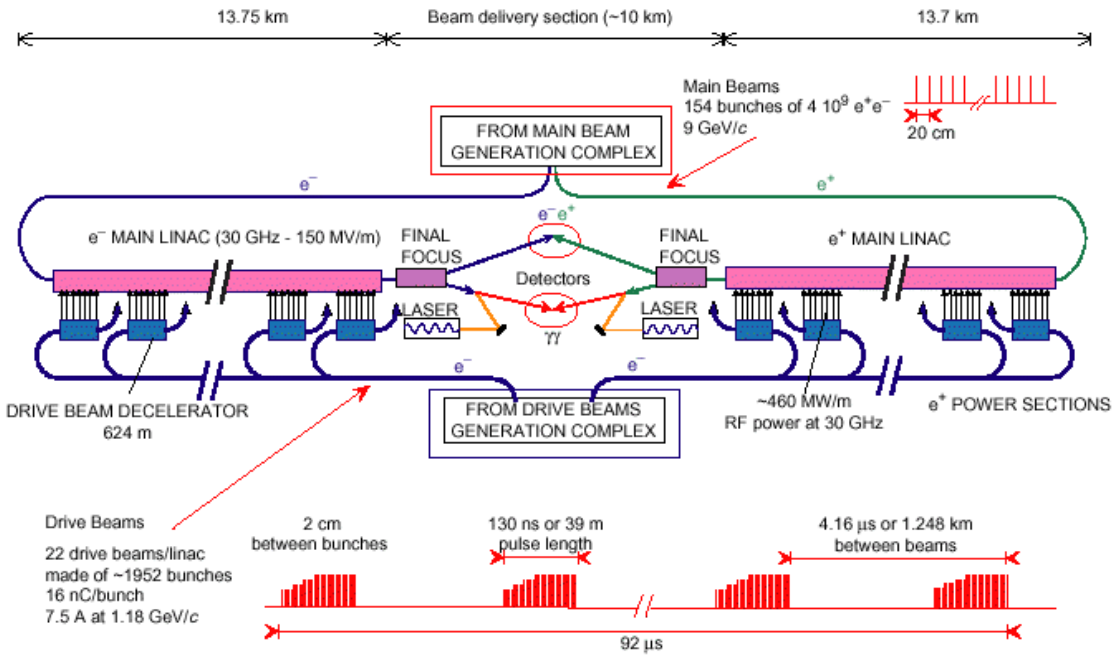



**Figure 1.3:** Overall layout of the CLIC for the centre-of-mass energy of 3 TeV [16].

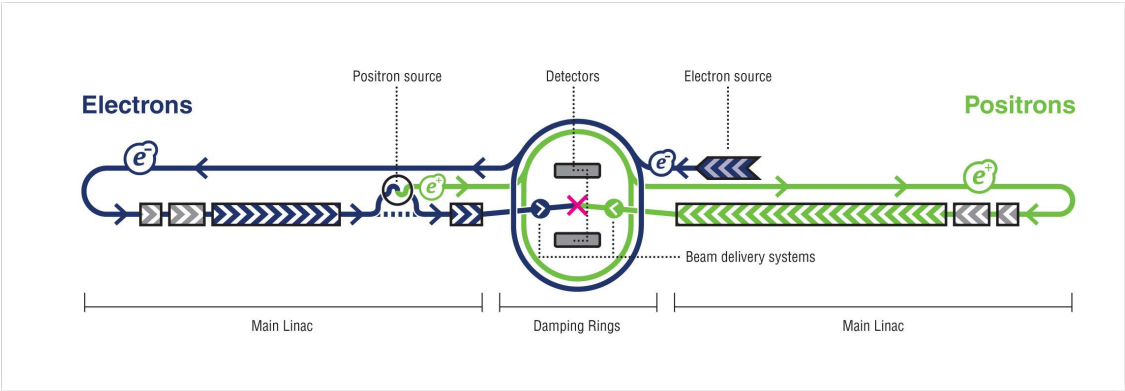



**Figure 1.4:** Overall layout of the ILC [18].

by the electromagnetic waves up to a center-of-mass energy in the range of 0.5 TeV. The ILC layout is shown in Fig. 1.4. This schema presents the electron and positron beams, their sources, the accelerating pipes (Main linacs) and the damping rings as well as the placement of the detectors and the interaction point.

The CLIC and ILC Collaborations agreed to join their resources, knowledge and efforts within the framework of the CLIC/ILC Collaboration in order to co-operate

on common issues, such as detector performance studies, R&D on sub-detectors, and software tools.

### 1.3.1 Prospects for physics.

The $e^+e^-$ collider experiments are expected to provide an essential complement to the physics discoveries explored by the LHC, by increasing the precision. One of the main questions posed to the LHC is proving the existence of the Higgs boson — a particle, which would help to explain the origin of mass in the universe. CLIC would be a great vehicle to verify this possible discovery and measure subtle properties of the Higgs boson. Another example of physics requirements, is the supersymmetric model predicting that every particle in the Standard Model should be accompanied by a supersymmetric partner typically with a mass smaller than 1 TeV. Alternatively, theories with extra spatial dimensions predict new particle excitations or other structural phenomena at the TeV scale. Alternatives to the Higgs boson, such as new strong interactions, could also be observed. It is expected that the experimental conditions of CLIC will allow for many detailed measurements, complementary to the LHC and ILC, which for example cannot provide a complete investigation of properties of the Higgs boson in case it is a relatively heavy particle. A more detailed study about the physics potential of CLIC can be found in Ref. [19].

### 1.3.2 Overview of the detector system.

The studies of detector systems are influenced by experience gained at LEP and by technical solutions being adopted for the LHC [19]. Nevertheless, to fully exploit the physics opportunities presented at CLIC and ILC, it is necessary to develop a detector system with capabilities far beyond the detectors at LEP and LHC. The detector systems for linear lepton colliders does not need to cope with extreme data rates or high radiation fields, but they need to achieve unprecedented precision to reach the performance required by the physics [20]. Therefore, much higher performance of the CLIC/ILC detectors in comparison to the ones used at LEP and LHC means much better jet energy resolution, tracker momentum resolution and impact parameter resolution of the vertex detector.

Although the ILC and CLIC are based on different concepts, one area of common interest is the development of suitable detectors for the particular environment of a TeV scale $e^+e^-$ linear colliders. Therefore, the focuses on physics and detector system issues for future $e^+e^-$ collider has been established within the ILC-CLIC collaboration [21].

Concepts of the ILC detector system are the subjects of the Detector Concept Report (DCR) [20] published in 2007. They are based on the combination of an excellent precision and low mass tracking system and a calorimeter with very fine transverse and longitudinal segmentation. Since the progress of R&D in ILC case is more advanced, the commonly investigated solutions driven by the CLIC collaboration, are based on ILC concepts, namely the International Large Detector (ILD) [22] and the Silicon Detector (SiD) [23]. Both concepts are built on silicon based tracking: multilayer pixels for the vertex detector and a system of strips and pixels for tracking purposes. Excellent tracking and calorimetry has to be combined to obtain the best overall event reconstruction capability. Despite the basic concept of the detectors being similar for both projects, there is a large number of areas, where the CLIC and ILC represent different specification, originating from the two following differences between both projects:

– the energy of collided beams; up to 1 TeV for ILC and up to 3 TeV for CLIC,

– the time structure of the accelerators; train repetition rate for ILC will be 5 Hz, each train will contain 2820 bunches separated by 337 ns. CLIC's train repetition rate will be 50 Hz, where single train is composed of 312 bunches, 0.5 ns apart.

Higher beam energy as well as more frequent particle collisions in CLIC drives its detector and readout electronics in a path, which differs from the ILC design. Therefore, the initial CLIC concept simulations and studies as well as CLIC oriented R&D are required in many technological areas, especially the development of the detectors and readout electronics technologies and architectures. A brief description of the CLIC vertex detector concepts currently under study is presented further in this chapter. One of the pixel detector technologies being investigated for CLIC vertexing purposes is presented in detail in Chapter 3.

## 1.4 Tracking detectors in future High Energy Physics experiments.

For many years, the tracking systems in particle colliders have been based on silicon detectors, which provide an accurate position measurements due to high density micron-scale sensors that can be produced as large area crystals of 10 to 15 cm diameter. Silicon sensors are based on well established technologies, which have become cheaper over the past years, allowing for the construction of feasible and affordable large-area trackers.

One can easily form strip or pixel shapes in order to provide spatial resolution, of the order of 10 μm [24] in one or two coordinates. Fast charge collection of about 8 ns for electrons and 25 ns for holes in standard, 300 μm thick fully depleted silicon sensor [25] is another indisputable advantage, which makes the silicon sensor technology suitable for tracking purposes. Nevertheless, future HEP experiments put challenging requirements on the tracking systems, which can be categorized as follows:

1. Spatial resolution of the vertex and tracking detectors needs to be improved. The precision of track reconstruction is mainly determined by the sensor size and by the incident angle of the particle crossing the sub-detectors. In order to obtain a precise measurement of the impact parameter, high resolution of the innermost detectors is of primary importance. This is mainly limited by multiple scattering on the quantity of material crossed by the particle. Therefore, the overall material budget of the system — its inner layer at least — needs to be reduced while maintaining noise performance, precision and speed. In particular, for the innermost pixel layers the standard silicon wafer thicknesses of 300 μm is too much given the material budget limitations of both, the CLIC and S-LHC experiments. Therefore new detector concepts are being investigated to meet the discussed requirements.

2. The radiation tolerance of the present sensors has to be improved. This is the case for the S-LHC, where the fluence is foreseen to reach up to $1 \times 10^{16}$ $n_{eq}cm^{-2}$ in the innermost layer. This pixel layer requires either a new sensor technology or replacement every few years if employing currently available pixel technologies. The R&D study made by the S-LHC collaboration shows that high resistive *n*-type silicon substrates can cope with fluencies of several times $10^{15}\,n_{eq}\,cm^{-2}$, which is sufficient for outer pixel layers at radii larger than about 10 cm [11]. In the CLIC environment, the expected fluencies are a few orders of magnitude lower than for the S-LHC case, about $10^{10}\,n_{eq}\,cm^{-2}$ per year [26].

3. Finer granularity of detectors is required to handle higher particle fluxes and to reduce the influence of overlapping events.

4. Interconnections between the sensors, front-end readout electronics and the back-end systems need to be improved in order to cope with larger number of channels and to decrease the material budget.

5. Cooling techniques of the silicon strip and pixel detectors need to be studied and improved. For example, current LHC trackers' cooling system does not fulfill the

material budget constraints of CLIC. The needs of cooling for S-LHC are still under investigation. Reducing the power consumption in the front-end electronics will help to solve the cooling problems.

6. An affordable cost for the tracker is an important aspect to be taken into account in the design, since the large-area trackers are foreseen to reach tens to hundreds of square meters of active sensor area.

Taking into account the requirements listed above, two tracking detector concepts for the S-LHC and CLIC experiments are presented in the following Section 1.4.1 and Section 1.4.2, respectively. The work presented further in this thesis has been performed by the author as contributions to the R&D projects on these two tracking detectors.

### 1.4.1 Silicon strip detectors for the upgraded ATLAS Inner Detector.

An increased luminosity of the S-LHC machine results in major changes in the ATLAS experiment. In particular, the whole Inner Detector will be replaced by an all silicon tracker [27] (see section 1.2.2). The layers at radii larger than about 30 cm will be made in silicon strip detector technology that can operate up to fluence of $10^{15}\,n_{eq}\,cm^{-2}$. In order to ensure efficient tracking and low detector occupancy under high track density per bunch collision. it is required to obtain much finer detector segmentation than the one employed in present ATLAS Semiconductor Tracker. Furthermore, while the SCT for ATLAS was designed for a fluence of $2 \times 10^{14}\,n_{eq}\,cm^{-2}$, the fluence levels for the tracker upgrade are about five times higher. Thus, it becomes clear that SSD developed for the SCT will not stand the S-LHC environment due to excessive radiation damage.

The bulk damage induced by radiation in the detector material results in displacement damage in crystal lattice, which acts as deep energy levels in the energy gap of the silicon. These damages result in the following effects [28]:

1. Increase of leakage current resulting in higher power dissipation and an increase of electronics noise. Furthermore, exponential rise of the leakage current with temperature invokes a catastrophic thermal behavior, called thermal runaway, in which the detector module is heating up itself abruptly once it goes beyond a critical temperature [29]. This effect can be limited by keeping the detector in sufficiently low temperature, however this introduces additional complication to the cooling system.

2. Changes of effective doping concentration caused by an increase of acceptor-like defects. This results in inversion of the *n*-type substrate into a *p*-type substrate beyond radiation fluences of a few $10^{13}\,\mathrm{n_{eq}\,cm^{-2}}$. Then, in the *p*-type strips in *n*-type substrate (*p*-on-*n*) sensors, the detector junction moves from the strips side to the ohmic contact side, from where the depletion region is built-up and it extends towards the strip side. While operating the sensor in partial depletion, the collected charge has to cross a non-depleted region, where most of it is lost through recombination before reaching the electrodes [30], providing a very low signal to the readout electronics. In the current SCT, the *p*-on-*n* detectors have to be operated in the over-depleted state, to allow efficient charge collection beyond the fluencies causing substrate type inversion. An expected full depletion voltage for these detectors after the S-LHC fluence of $10^{15}\,\mathrm{n_{eq}\,cm^{-2}}$ is around 2000 V, which is not a realistic operation point [31]. Thus, the S-LHC environment requires a new approach for strip-shaped sensors to be used in upgraded ATLAS ID.

3. Increase of charge trapping due to lattice damage. If the charge carriers, electrons or holes, are captured and their re-emission takes longer than the shaping time of the readout electronics, the trapped charge carriers do not contribute to the sensed detector signal and thus the charge collection efficiency is reduced. In order to reduce the trapping, the choice of detectors which collect electrons has some advantage due to higher saturation drift velocity compared to holes.

The technologies, in which the signal is read out at the $n^+$-side of the sensor, are $n^+$-on-*n* and *n*-on-*p*. The former one requires photolithographic processing on both sides of a wafer in order to implement the $n^+$-side readout in *n*-type substrate, increasing the cost of manufacturing by about 50% [28]. Because of the large total area of tracking detectors, the cost of sensor fabrication is an important factor. This fact leads to a choice of single-side-process *n*-on-*p* sensors. The *n*-on-*p* sensors have a significant advantage in comparison to the *p*-on-*n* ones, employed in current SCT, namely, no junction migration takes place on *p*-type silicon substrate and the depletion region is always in contact with the *n*-type strips. Hence, the operation of partially depleted detectors is feasible, avoiding the need for very high biasing voltages. Then, the signals generated in SSD are smaller than for a fully depleted sensor, despite being compensated by lower electronic noise resulting from smaller strip size in the inner layers. Furthermore, the reading out of the strips is performed on the *n*-type side of silicon junction that collects electrons, which are faster carriers than the holes in silicon . Thus, the signal loss due to under-depletion

is partially compensated. In addition, faster charge collection time reduces the ballistic deficit effect, which manifests itself as the loss of the signal amplitude at the pulse shaping circuit output due to non-negligible charge collection time in comparison to pulse shaping time (see Ref. [32] for more details on the ballistic deficit effect).

More details on the prototype SSD and its readout electronics for the upgraded ATLAS ID, is presented in Chapter 2.

### 1.4.2 Vertex detectors for CLIC.

The technologies suitable for a CLIC vertex detector are subjects of the ongoing CLIC R&D program [21]. In order to take full advantage of the physics potential provided by CLIC, a vertex detector concept, which optimally combines high detector resolution and efficiency with satisfactory background suppression capabilities, needs to be developed. The vertex tracker will consist of multilayer barrel section surrounding directly the beam pipe and is complemented by forward discs to ensure tracking down to small angles. Each layer will be segmented into very small pixel cells, composed of the sensor and its readout electronics [19]. Although, the final requirements concerning the sensor parameters have not been set yet, preliminary assessments can be found in [33], [34] and [35].

The need for high resolution in the impact parameter of tracks puts stringent requirements on a single point resolution, as well as on the multiple scattering of the particles in the detecting system volume. The spatial resolution of 10 μm is presently obtained by pixel detectors with 50 μm pitch developed for the LHC. In order to provide the high precision of track measurements and accurate characterization of full vertex topology for particle production and decays at CLIC, the spatial resolution of few micrometers is required. The most recent specification aims at the single point resolution of about $3-5$ μm[35] and according to [36] the target for pixels pitch is 20 μm.

The limitation of multiple scattering can be accomplished by minimizing the amount of material in the active volume, aiming at single-layer material thickness of 0.1–0.2%$X_0$, where $X_0$ is the radiation length. This material budget aims at factor about 10 time less than in the LHC for the central region and about 100 for the forward region. Therefore, the detector thickness, level of system integration, mechanical and cooling system complexity are the issues, which have to be taken into account.

The vertex detector is the closest layer to the interaction point, thus it has to cope with high occupancy due to background hits. The major source of the background are the electron-positron pairs, which are created in a great number in the interaction of

primary electron and positron bunches as well as secondary particles originating from the $e^+e^-$ pairs interaction with detector and machine components. The second important background component comes from the "beamstrahlung" photons. Other potential background sources are under investigation in order to find the trade-offs between boosting the energy and luminosity of the beam and enhancing the tolerance of vertex detectors to the resulting backgrounds. The best case would be to place the first vertex layer just next to the beam-pipe to improve the impact parameter resolution for the middle and low momenta particles, which depend on the thicknesses of both, the beam-pipe and first vertex layer, as well as their distance form the interaction point. Nevertheless, the high background rates as well as the limited radiation immunity of the detector and its readout electronics cause pushing the vertex layers further from the beam-pipe. These trade-offs are currently being investigated. The maximum occupancy at maximum energy of 3 TeV and luminosity of $6 \times 10^{34} \mathrm{cm}^{-2}\mathrm{s}^{-1}$ is aimed at 1% including a safety factor of about three [36]. The vertex detector is required to handle the sensor efficiency reduction due to bulk damage inducted by neutron flux, possibly in the order of $10^{10}\,\mathrm{n_{eq}\,cm^{-2}}$ per year [19]. As it was mentioned in Section 1.4.1, current silicon-based technologies are robust enough and can easily operate in such environment.

Another issue to be handled by the vertex detector is timing requirements related to particle train time structure and a train repetition rate of 50 Hz. If the detectors are not fast enough to time-stamp the individual bunch crossings, just a full bunch train or a large part of it, then the background of many bunch crossings will be accumulated. This results in the need for an innermost tracker layer with sub-nanosecond time resolution, in order to distinguish individual or several bunch crossings [33].

In order to fulfill the challenging requirements of CLIC vertex detectors, present pixel technologies need to be further improved, as listed below [19]:

1. Charged Coupled Devices (CCD) [37], [38] provide high segmentation and point resolution better than $4\,\mu$m, as well as thin sensors with thickness about $20\,\mu$m. Although two limitations remain: low readout speed and sensitivity to neutron radiation damage.

2. Hybrid Pixel Sensors (HPS) [39] successfully developed for the LHC program are sufficiently radiation hard and can be read out rapidly. A single point resolution of $3\,\mu$m can be achieved if tracks are sufficiently isolated. Nevertheless, HPS needs to be developed as much thinner devices with a smaller cell size, to improve their spatial resolution of multi-jets.

3. Monolithic Active Pixel Sensors (MAPS) [40] provide a good spatial resolution of 2 μm and low layer thickness thanks to small pixel size and electronics integrated on the same silicon wafer as the sensor. Its tolerance to neutron fluxes has been proven as sufficient for the linear colliders environment, but the readout speed and functionality of the front-end electronics need to be improved.

In parallel, novel solid-state detector technologies are studied as potential candidates for CLIC vertexing purposes. One of them is 3D silicon sensor [41], [42], where the three-dimensional array of electrodes, typically with pitches at a few tens of microns, penetrate the detector from one surface through most or all of the bulk. The advantage of these structure include short collection time, low depletion voltages and short collection distances set by the electrode spacing rather than the substrate thickness which is the case in conventional planar technology. Another option, called DEPleted Field Effect Transistor (DEPFET) structure, is the realization of Field Effect Transistor (FET) devices integrated in high-resistivity fully depleted *n*-type bulk, which amplifies the charge at the point of collection [43]. The advantage of DEPFET structure are its low input capacitance, which allows achieving low noise, and the large sensitive volume, where the maximum signal for given thickness can be achieved due to full depletion of the structure [44].

The next attractive architecture is a monolithic pixel detector based on Silicon-On-Insulator (SOI) technology [45], [46]. In this technology the CMOS front-end circuitry is fabricated on top of a thin silicon-oxide layer, which is placed on the surface of a high-resistivity silicon substrate. This structure combines the advantages of a fully depleted sensor and of a monolithic structure, which allows to reduce the total sensor thickness. Furthermore, both P-type and N-type Metal-Oxide-Semiconductor (PMOS and NMOS) transistors can be implemented in the readout channels, hence more sophisticated CMOS circuitry can be integrated in each pixel cell.

Another important candidate for the vertex detector in CLIC experiment is a Thin Film on ASIC technology, where the sensor is made of hydrogenated amorphous Silicon (a-Si:H) [47], [48]. This sensor is thin, up to 30 μm, provides good resolution, fast response and sufficient radiation tolerance. The high level of sensor integration with its readout electronics is provided at low manufacturing cost. The TFA technology,which is one of the subjects of this thesis is discusses in detail in Chapter 3, with emphasis on the readout electronic.

## 1.5 Front-end electronics for the future tracking detectors

In large tracking systems, the sensors and the readout electronics are aimed to be low mass in order to reduce scattering, low noise, fast response, low power and radiation tolerant. The main requirements and trade-offs, which are posed to the readout electronics in the ATLAS ID Upgrade and in the CLIC vertex detector, are described further in this section. The architecture and functionality of two front-end circuits, are presented in Chapter 2 (ATLAS Upgrade) and in Chapter 3 (CLIC). The key issues are listed below.

1. A large rate of physics events together with detector occupancy restrictions affect directly the granularity of sensors and the number of electronic channels. This puts quite harsh constraints on the space taken by the readout electronics, its power distribution and a number of readout links. The space available for the power cables and other services, like cooling and support structures, is limited, and thus an efficient power distribution scheme appears as one of the critical problems to be worked out [49]. Furthermore, an incoming event rate puts the demands on speed of the front-end electronics, which influences the power dissipation as well as requires the back-end electronics and output links for data communication to handle very high data rates in available space.

2. The radiation tolerance is a concern for very few applications, like HEP, nuclear power industry and space missions. This makes the radiation-resistant electronic components unavailable to be bought off-the-shelf. For this reason front-end electronics for future HEP applications needs to be carefully designed using proper architectures and layout techniques improving their radiation tolerance [50], in order to ensure the correct functionality of the circuits at high fluencies environments over a many years. Development of the electronic systems has to be carried out using the radiation-hard technologies, which are not only cost effective, but also available now for R&D and in the future, when the detector systems will be constructed in their final shape. The research made on deep sub-micron and nano CMOS technologies, 130 nm and below, shows that they are suitable for operation at very high radiation level in the tracking systems.

3. Efficient particle detection requires a sufficient Signal-to-Noise Ratio (SNR). The amount of signal charge, which is read out, depends on many parameters, like

sensor material, its thickness, segmentation, sensor bias voltage, etc. Thicker detectors deliver larger signals and present a smaller input capacitance to the front-end electronics improving its noise performance. This capacitance depends also on the sensor material and the single cell area — the bigger the size, the higher the capacitance. The geometry and arrangement of the sensors is also important, as the single detector cells introduce parasitic capacitance to its neighbors, which may result in crosstalk, as well as an increase to total input capacitance of the readout electronics, worsening its noise performance.

These aspects are not independent of each other, and thus their correlations should be kept in mind while searching for the trade-offs. For example, reducing the thickness of the sensor results in lower signal delivered to the readout electronics and higher input capacitance to the front-end electronics, what degrades SNR. Furthermore, in order to ensure low noise levels, more power is needed, increasing the mass of cables supplying the readout electronics and of the cooling system. Low noise of the front-end electronics increases the margin for the radiation tolerance of the system, since the SNR is maintained while the signal level decreases in irradiated sensors. The noise generated due to the detector leakage current can be reduced by faster shaping of the signals. However, it costs an increase of the voltage noise and the higher power consumption. In parallel, an increase of the speed of the front-end electronics is limited, because it implies an increase of the power consumption, which should be minimized for multichannel and complex system. Therefore, a sufficient segmentation needs to be provided, which reduces the event rate per channel and decreases the front-end input capacitance, resulting the lower electronics noise and lower detector leakage current.

As it can be seen, it is necessary to take into consideration all these conflicting requirements in order to properly optimize the performance of the sensor and its front-end electronics. In tracking systems for HEP experiments, one needs to have a global overview of the system. Since the HEP readout circuits are the full-custom designs, the number of issues at all the design levels have to be handled. Starting from an optimization of a single transistor, going up in a design hierarchy through the analog and digital building blocks providing a single detector readout channel; then combining certain amount of readout channels in a single chip and further assembling of several chips to build modules, which are the basics bricks of a large detector systems. Therefore, precise design of a single cell would be worth nothing without a concept of grouping the detecting cells into modules, and then constructing the required system geometry. The detector cooling system, the data links and power cables and the support structures need to be taken into account. All these

designs depend of course on the available financial budget, for which these trade-offs need to be accomplished. Despite great knowledge delivered by R&D on silicon detector readouts for the LHC experiments, the S-LHC and CLIC environments push further the development of front-end electronics, which is the main aim of this thesis.

# Chapter 2

# The ATLAS Inner Detector Upgrade

The luminosity upgrade of the LHC poses significant challenges to the ATLAS and CMS experiments [5]. The target of the ATLAS Inner Detector Upgrade program is to prepare a design, which can operate up to 10 times higher radiation doses, compared to the current ID, and can cope with much higher particle fluxes, as mentioned in Section 1.2.2. As a consequence, the requirements of new radiation-hard technologies and a finer granularity are posed to the detectors, in order to keep the hit occupancy acceptably low and maintain good pattern recognition of particle tracks in the SLHC environment. The new ID will consist of a vertex region, composed of the pixel detectors, and the tracker region, built of short strip and long strip silicon detectors, as discussed in Chapter 1 (see Fig. 1.2).

An intensive R&D program is underway to develop silicon sensors robust enough for an integrated luminosity of 6000 $fb^{-1}$ — including a factor of two safety margin — and with sufficient granularity to keep the detector occupancy below 2%. It has been shown [11],[51],[52], that the *n*-on-*p* silicon strip detectors, consisting of *n*-type strips processed on *p*-type bulk, is the most suitable technology to be implemented in the tracker region of upgraded ID. The *n*-on-*p* SSD structures are briefly discussed in Section 2.1 of this chapter.

The necessity for higher detector granularity implies an increased number of electronic readout channels. For the upgraded ID it is foreseen to cope with 5 to 10 times more readout channels than the ID in present ATLAS detector. Thus, the power consumption of the readout chip is one of the most critical issues; on top of the other usual requirements concerning noise, timing parameters and radiation hardness. All these requirements have to be considered, taking into account the present and expected trends in development of industrial CMOS processes. In order to build a realistic prototype

detector module, one needs to develop first a readout chip with full functionality and parameters close to the final ones, as required for the ID Upgrade. For this reason, a R&D proposal has been initiated, aiming at the development of a new ASIC for the ATLAS Semiconductor Tracker Upgrade [49].

The architecture and functionality of the ABCN-25 chip are described in Section 2.2. Special attention is paid to the analog part of the ASIC, primarily to the front-end electronics, calibration circuitry and the digital-to-analog converters. The initial evaluation test results of prototype ASIC are presented in Section 2.3. The development of the ABCN-25 chip is concluded in Section 2.4.

## 2.1 Silicon strip detectors for the ATLAS Inner Detector Upgrade

**Principles of silicon strip detector structure**

A strip detector is an array of reverse biased $n^+p$ diodes, where strip like shaped $n^+$ implants are placed on a common high-resistivity $p$-type silicon wafer. The strip pitch is the main geometrical parameter, which determines the detector spatial resolution. The schematic structure of a single-sided $n$-on-$p$ silicon strip detector is presented in Fig. 2.1.

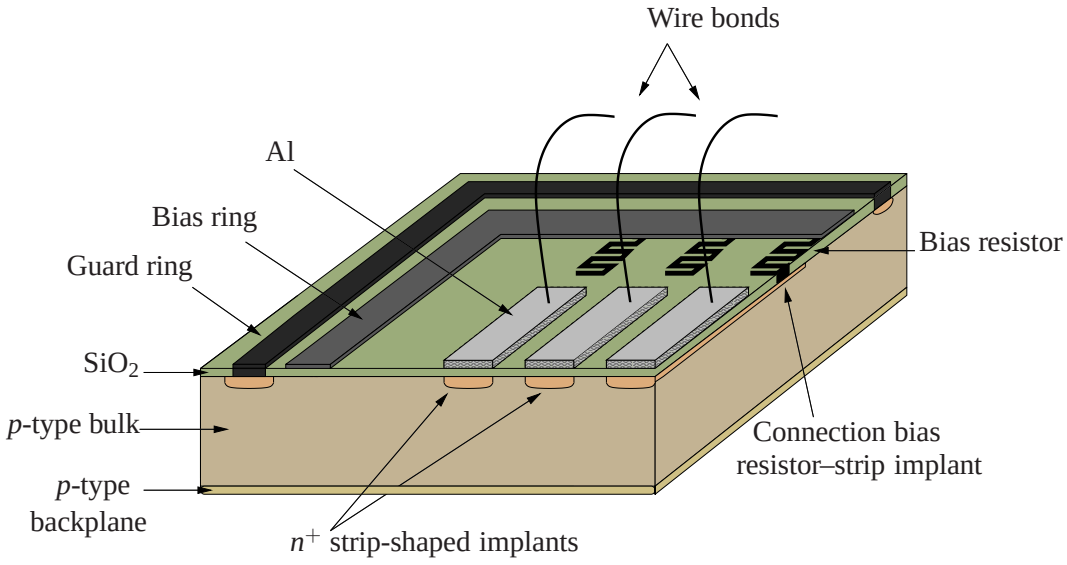



**Figure 2.1:** Schematic structure of $n$-on-$p$ SSD

Each $n^+$ strip is separately biased through the polysilicon bias resistor connected to the common bias ring surrounded by a guard ring. The depletion zone of the reverse biased $n^+p$ junction acts as the detection volume, whose depth depends on the bias voltage $V_b$ and the bulk effective doping concentration $N_{\text{eff}}$. The bias voltage necessary to fully extend the depletion zone throughout the detector thickness $d$, is called the full depletion voltage $V_{\text{dep}}$, and is defined by Eq. 2.1

$$V_{\text{dep}} = \frac{q}{2\varepsilon\varepsilon_0}|N_{\text{eff}}|d^2, \tag{2.1}$$

where $q$ is the electron charge, $\varepsilon$ is the vacuum dielectric constant and $\varepsilon_0$ silicon relative dielectric constant.

A high energy charged particle while traversing the semiconductor detector volume, deposits energy along the track, producing mobile charge carriers: electron-hole (e-h) pairs. The amount of created e-h pairs is proportional to the energy absorbed in the sensitive volume. The electric field in the sensor separates the generated charge carriers, causing their drift — electrons towards the $n^+$ strips side, and holes towards the $p^+$-doped back side of the detector. While the electrons and holes are drifting towards the electrodes, the current is induced on the anode and cathode, respectively. The induced current signal is sensed by the electronic circuits connected to each strip. There are two ways of connecting the detector to its readout electronics - Direct-Current (DC) coupling, and through a coupling capacitor, called Alternate-Current (AC) coupling. In the second option, the coupling capacitor is implemented as $n^+$ implant–insulator ($SiO_2$)–strip-shaped metal structure, where insulator is common layer for all the $n^+$ implants, and each metal strip is separately connected to the readout electronics by a wire bond.

The DC-coupled SSDs have few advantages in comparison to AC-coupled structures, namely no oxide layer is placed on the $n^+$ implants, which in the AC-coupled detectors causes problems with reliability and breakdowns. In addition, the DC-coupling requires less masks, less processing steps during manufacturing and has less dead area in the detector volume, since no biasing resistors for the strips are needed. However, DC-coupled devices introduce detector leakage current to the front-end circuitry. In order to keep the proper operating points of the preamplifier, an additional circuit which compensates the detector leakage current has to be implemented. This imposes an increased complexity on the readout ASIC as well as introduces an additional noise source in the preamplifier, which can become significant for very high detector leakage currents

originating form sensors exposed to heavy radiation damage. The motivation of using AC-coupled SSDs in the ATLAS SCT Upgrade is presented in details in [53].

### 2.1.1 The *n*-on-*p* silicon strip detector for the ATLAS Inner Detector Upgrade

As mentioned in the previous chapter, the *n*-implant strip in *p*-type wafer is an advantageous option to be implemented in the upgraded ATLAS silicon strip detectors. The main benefits are:

– the acceptor-like defects generated in the irradiated substrate do not invert the dopant type of the substrate, which is the case for *n*-type wafers,

– single-side lithography process is more cost-effective than double-side processing like *n*-on-*n*,

– sensors can operate partially depleted after accumulation of high fluencies, since the depletion zone of the *p*-*n* junction builds up from the readout strip side,

– the readout is based on collecting electrons, thus the charge collection is faster and less charge is trapped.

One of the technological challenges of manufacturing the *n*-on-*p* detectors is keeping good separation between the strips, otherwise they may be short-circuited together by the electron accumulation layer, which is induced on the silicon-oxide interface by the positive charge accumulated in the $SiO_2$. Therefore, the surface barrier structures, which interrupt the inversion layer, are formed by implanting *p*-type dopants in restricted areas (called *p*-stop). However, the *p*-type barrier structures, together with *n*-type implants and high bias voltages, cause high local electric field, which leads to the onset of microdischarge if the electric field strength exceeds the avalanche breakdown voltage of about $30\,\mathrm{V\mu m^{-1}}$. This increase of the leakage current can be avoided by adjusting the concentration of *p*-type dopants, for which the onset voltage of the microdischarge is kept above the operation voltage. In the past few years, the *n*-on-*p* strip sensors have been developed and tested [11],[51],[52], in order to prepare the SSD design suitable for the upgraded ATLAS tracker. The specification of the radiation-tolerant silicon strip sensor for the upgraded ATLAS Inner Detector, as published in Ref. [54], is listed in Tab. 2.1.

## 2.2 Front-end electronics for the ATLAS Semiconductor Tracker Upgrade

The prototype ASIC, called ABCN-25, has been designed in a 0.25 μm CMOS technology. The front-end design has been optimized for the short, 2.4 cm, silicon strips foreseen in the middle layer of the upgraded ATLAS Inner Detector. The ABCN-25 prototype is considered as an intermediate step towards implementation of this readout architecture in a more advanced process for the final design. Reasons for implementing the present prototype in the 0.25 μm CMOS technology were partially economical and partially technical, concerning the availability of design kit tools.

All the critical aspects of the new architecture have been implemented in the present prototype, therefore this ASIC is used as a basic test vehicle in the development of the detector modules for the ATLAS SCT Upgrade. The ABCN-25 chip provides all the functions required for processing the signals from 128 silicon strips, namely: integration, amplification, noise filtering, zero suppression and sparsified readout. Various schemes for power distribution, like serial powering of modules or DC-DC step-down converters on the detector, are under investigation [55] in order to minimize the number of cables as well as reduce the material in the detector volume and increase the power efficiency. Thus, the new ASIC architecture is compatible with whatever power distribution scheme will be adopted in the future. There are two other issues driving development of the front-end electronics, namely the availability of a suitable and affordable technology and its radiation hardness. It has been demonstrated that submicron CMOS processes (e.g. 0.25 μm) can offer radiation hardness up to tens of Mrads after applying special layout hardening techniques [50]. Using technologies with a smaller feature size

**Table 2.1:** Specification of the radiation-tolerant silicon strip sensor for the upgraded ATLAS Inner Detector.

| | |
|---|---|
| Silicon wafer diameter | 6-inch (150 mm) |
| Silicon wafer resistivity | $\geq$4 k$\Omega\cdot$cm |
| Silicon wafer thickness | 320 μm |
| Strip pitch | 74.5 μm |
| Strip length | 2.39 cm |
| Interstrip capacitance | 0.80 pF/cm |
| Body capacitance (to the backplane) | 0.27 pF/cm |
| Bias resistor (Polysilicon) | 1.5 M$\Omega$ |
| AC coupling breakdown voltage | $\geq$100 V |

(e.g. 0.13 μm) may result in better radiation hardness; so that one can avoid using transistors with enclosed gate geometry layout, which are highly area-consuming. In addition, the transistors with enclosed gate geometry have higher capacitances which result in speed limitation and higher power consumption of digital circuits. With a smaller feature size the power supply voltage becomes lower, offering the possibility of power savings compared to currently used technologies. However, very low power supply voltage, for example 1.3 V for. 0.13 μm processes, is very challenging for designing analog circuits.

### 2.2.1 Requirements and functionality of the ABCN-25 chip

The basic concept of the ABCN-25 follows the architecture of the ABCD3T ASIC implemented in BiCMOS[1] DMILL[2] technology and used in the present ATLAS SCT detector [56]. A block diagram of the ABCN-25 is shown on the Fig. 2.2. The core of the binary readout architecture includes:

1. 128 front-end amplifiers;
2. 128 comparators;
3. Input register;
4. Two levels of data buffering;
   (a) pipeline for trigger latency,
   (b) derandomizing buffer,
5. Block of Digital-To-Analog Converters, threshold and calibration control circuit;
6. Data compression and data serializing circuitry;
7. Power management;
8. Readout control logic.

The ABCN-25 chip has to deal with a high volume of data delivered from the detector and to process them providing sufficient time resolution in order to assign correctly the

[1] Integration of Bipolar junction transistors and CMOS technology into a single integrated circuit device.

[2] Durcie Mixte sur Isolant Logico-Lineaire

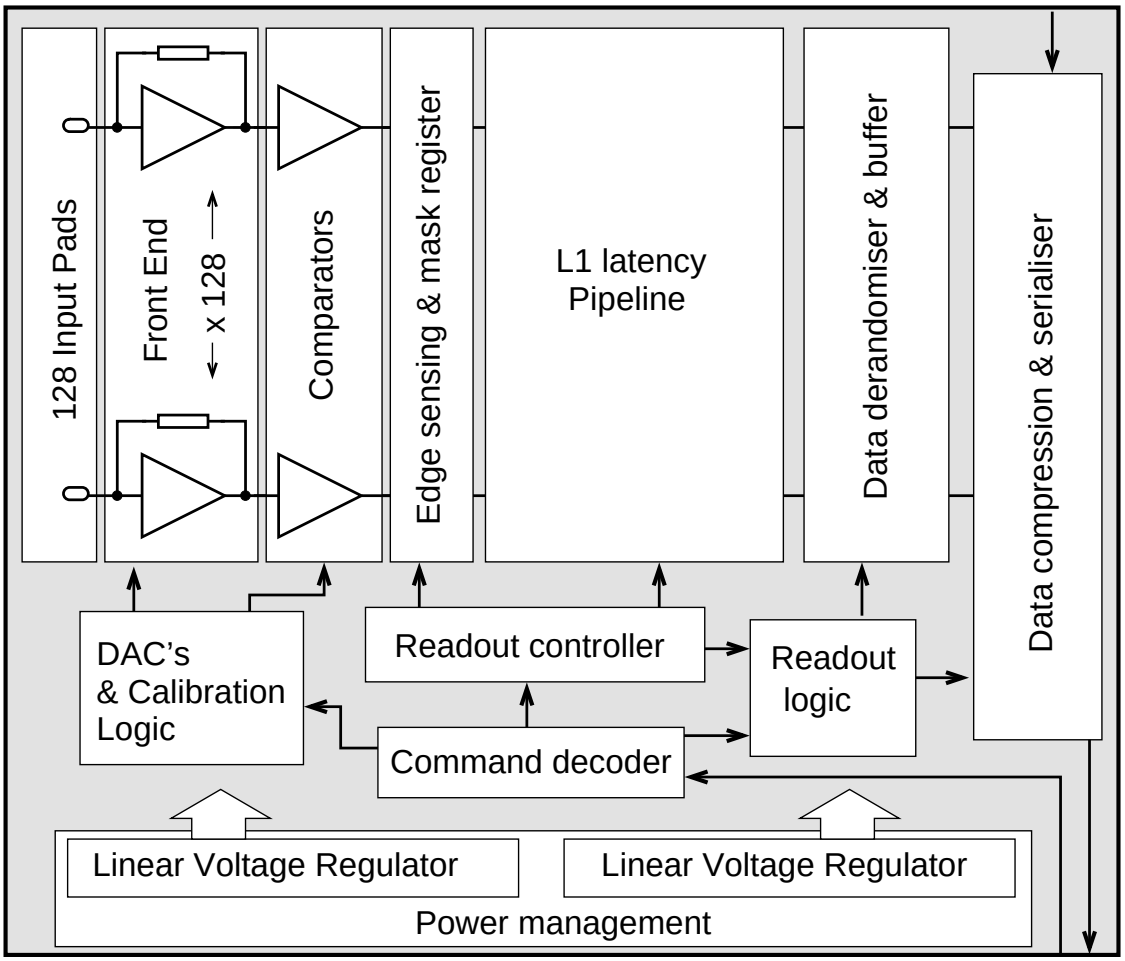



**Figure 2.2:** ABCN-25 block diagram.

data to given proton-proton collision. The front-end electronics has been optimized for 5 pF detector capacitance, corresponding to short strips of 2.5 cm, and it is compatible with either detector signal polarity. The signals received from the detectors are amplified, shaped and converted to binary signals at the comparator output. Due to large amount of data, transmitting the outputs associated with each bunch crossing from all the channels is impossible. The decision on which events are interesting from the physics perspective, is made in the calorimeters and muon spectrometers. This information is delivered with some delay to the tracker front-end electronics as a *trigger level one* (L1) signal. The data delivered by the comparators need to be kept on-chip until the L1 signal arrives to the front-end chip, therefore 1-bit yes/no information are stored in a 256 bits long pipeline, corresponding to a 6.4 $\mu$s latency time. Upon receiving the L1 signal the data is copied to the readout buffer, which acts as a derandomizing buffer. In the next step, the data is

compressed by applying a zero suppression procedure, then serialized and transmitted off the chip.

The ABCN-25 design includes on-chip power management circuitry to make it compatible with recent developments in the area of power distribution for the ID Upgrade, namely parallel powering combined with DC-DC conversion scheme and serial powering scheme. Each ABCN-25 chip contains two prototype power management circuits, which can be used alternatively [57].

One of the basic requirements addressed to the readout chips working in SLHC environment is the tolerance to ionizing radiation. Thus, the ABCN-25 prototype chip is designed in the IBM 0.25 μm technology, for which a radiation tolerance up to 100 Mrad total ionizing dose has been already demonstrated, provided special layout techniques have been used. Nevertheless, during the designing process, one cannot ignore the radiation effects in the front-end electronics. Thus, in order to prevent the disfunctionality of the analog circuits due to radiation effects, the special layout architectures and techniques, like enclosed geometry of the NMOS transistors and uniform biasing conditions for the matched transistor pairs, were used. An improve of the chip immunity to the Single Event Upset[3] (SEU) was reached by designing all configuration registers and the fast command decoder with triple vote logic and auto correction.

### 2.2.2 Front-end preamplifier design

#### Principles of front-end amplifier

Extraction of the detector signals is performed by the charge sensitive amplifier, consisting of an amplifier with a capacitor as a feedback element. The input charge is integrated on the feedback capacitor $C_F$, thus its discharge has to be provided, otherwise after several incoming pulses the amplifier output would be saturated. In general two reset methods can be implemented, namely a continuous or a pulsed one. The continuous discharge of the feedback capacitor is provided by a parallel feedback resistance $R_F$. Assuming an ideal amplifier of infinite gain $K_V$ and infinite bandwidth, the response of the circuit to a detector signal, approximated by the Dirac delta pulse, yields an output pulse of instantaneous voltage step decaying exponentially with a time constant $\tau_F = R_F \times C_F$, as presented in Fig. 2.3a.

[3]SEU is a change of logic state in the digital microelectronic circuit caused by ionization, that occures due to passage of single heavy ion close to a sensitive electronic element

The pulsed reset technique uses a programmable switch in the feedback, as shown in Fig. 2.3b. In the ideal case output signal consists of superimposed voltage steps while switch $S_R$ is open and exponential decay with time constant $\tau_F = R_{S_F} \times C_F$, when switch $S_R$ represented by resistance $R_{S_F}$ closes. Since the SLHC experiment brings high rates of data coming from the detectors, the continuous reset scheme has been implemented in the front-end preamplifier of the ABCN-25 chip. The pulsed reset approach has been implemented in the preamplifier of the AFRP chip [58],[59] and is further investigated in Section 3.3.

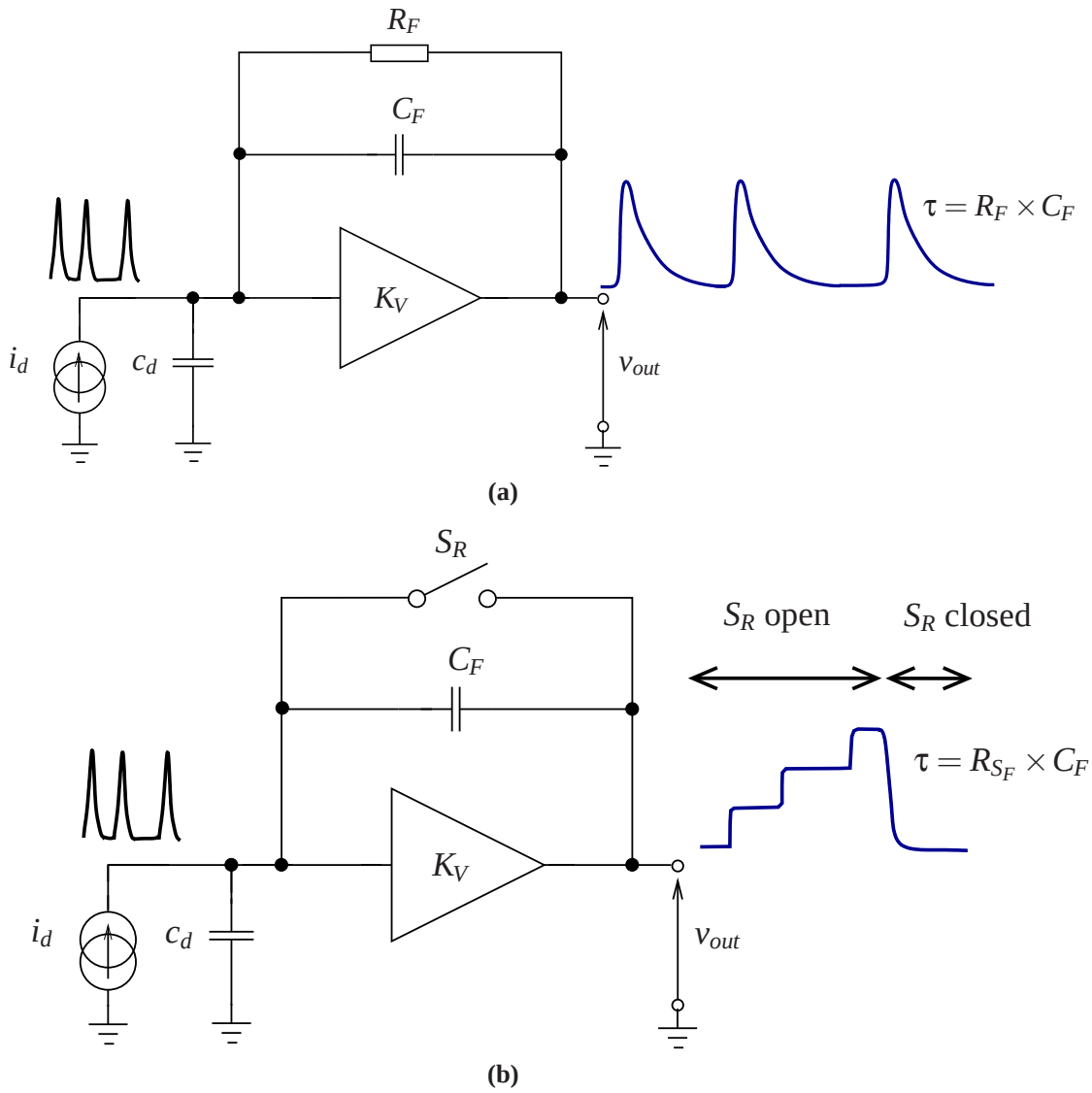



**Figure 2.3:** Schematic representation of charge sensitive amplifiers employing continuous (a) and pulsed (b) reset techniques.

The processes used for fabrication of deep submicron electronic devices do not provide precise passive components, in particular resistors. For example, in the 0.25 μm CMOS technology from IBM, the tolerances of low doped high-resistance polysilicon resistors are specified as $4100\,(+1770/-1230)\,\Omega$/square ($\Omega/\square$) [60]; what gives the ratio of maximum to minimum value above 2. Employing for example 100 kΩ resistor in the feedback loop of the transimpedance amplifier, together with a capacitor, which has a capacitance variation of about ±10%, would result in time constant variation from 16 ns to 40 ns for a nominal 25 ns value [53]. Since the time constant is one of the factors that determine the overall shaping function (and thus the peaking time and noise performance) its variation has to be minimized. Therefore, the amplifier architecture based on passive components is not suitable for front-end electronics to be implemented in the ATLAS ID upgrade. This fact is the main motivation for developing a scheme with an active feedback loop, in which the feedback passive resistor is replaced by a Metal-Oxide Semiconductor (MOS) transistor. In this architecture, the effective feedback resistance is adjusted by controlling the operating point of the feedback transistor. This way the process variation can be compensated, however, the current, which biases the feedback transistor, needs to be controlled by an additional transistor connected to the amplifier input node, hence introducing there an additional noise source. Furthermore, the feedback MOS transistor may present higher noise to the amplifier in comparison to a passive resistor of resistance equal to the equivalent resistance of MOS transistor, as a result of transistor excess noise (see Appendix B). Nevertheless, the active feedback architecture of the front-end preamplifier is still advantageous option in comparison to the one based on inaccurate passive components.

**Noise performance of the front-end transimpedance amplifier**

A schematic representation of the detector followed by front-end circuit including the equivalent noise generators are shown in Fig. 2.4. The main noise components are related to the shot noise of the semiconductor detector due to fluctuations of its leakage current as well as the electronic noise of the preamplifier. All noise sources influencing the signal being processed can be fully described by combination of current and voltage noise generators connected to preamplifier input, depicted as $e_{nt}$ and $i_{nt}$ in Fig. 2.4.
Noise of all resistors shunting preamplifier input are modeled as current noise generators, whereas noise of series resistors are represented by noise voltage generators. For this reason, the current and voltage noise sources are commonly called as “parallel” and “series” noise, respectively.

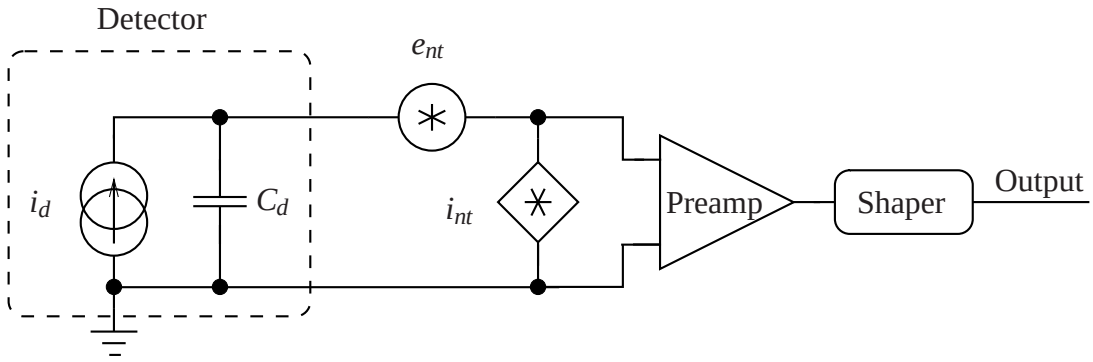



**Figure 2.4:** Schematic representation of the detector followed by the front-end preamplifier (Preamp) and shaper. The equivalent noise generators are depicted: $i_{nt}$ and$e_{nt}$ representing respectively parallel and series noise.

In order to increase signal-to-noise ratio of the front-end electronics, the preamplifier is followed by a filtering circuit. The filter reduces the bandwidth in frequency domain in order to attenuate the frequencies for which noise components dominate over the signal. This procedure shapes the signal profile in the time domain, hence filters are also called the shapers. The SNR factor can be maximized by applying so-called optimum filer, as described by the classical theory of noise filtering developed for nuclear spectroscopy systems [61],[62]. This however may require quite complex filter circuit, especially if applying time variant filters. Thus, the goals of lowering the power consumption and maintaining the simplicity of multichannel front-end electronics are the main reasons for implementing the continuous band pass filter, such as CR-$(RC)^n$ [63]. It consists of single differentiating stage, which filters out the low frequency noise components, and n-stages of integrators, which cuts off the high frequency components. One should keep in mind that the transimpedance amplifiers itself provides the CR-RC type signal shaping. This fact results form integration and differentiation of the signal are being provided by total capacitance connected to the input and by the feedback circuit, respectively. As an example, in the ABCN-25 chip the transfer function of transimpedance preamplifier and the filter can be approximated by a third order CR-RC filter — CR-$(RC)^3$.

In order to combine the noise performance and filtering capabilities of the preamplifier, the contribution of the system is commonly expressed as an Equivalent Noise Charge (ENC). ENC is defined as charge injected into the amplifier input as a Dirac impulse of current, that causes the voltage response, whose maximum equals the Root Mean Square (RMS) value of noise at the output. The ENC is a very useful parameter for comparing the electronic noise with the detector signals. Furthermore, the ENC depends not only on noise sources, but also on characteristics of the amplifier and the pulse shaper, as

expressed in Eq. 2.2 [25]

$$ENC = Q_N \sqrt{i_n^2 T_s F_i + C_i^2 v_n^2 \frac{F_v}{T_s} + C_i^2 A_f F_{vf}}, \tag{2.2}$$

where $i_n$ and $v_n$ are the spectral densities of the total series and parallel noise sources at the front-end circuit, $T_s$ is the shaper peaking time, $F_i$, $F_v$ and $F_{vf}$ are the noise factors depending on the shape of the output pulse, $C_i$ is the sum of all capacitances shunting the input and $A_f$ is a flicker noise coefficient. The first component of Eq. 2.2 describes the contribution of shot noise originating from the detector leakage current and from the thermal noise of the feedback resistor, or noise of the feedback transistor in case of active feedback in the preamplifier. The second component of Eq. 2.2 represents the contribution of white series noise source $v_n$, while the last term shows the contribution of $1/\mathrm{f}$ voltage noise. The parallel noise contribution increases with $T_s$, in contrary to series noise, which decreases while increasing $T_s$ for the white noise. The contribution of the $1/\mathrm{f}$ noise is independent of $T_s$. The peaking time $T_s$ is determined by the filter time constant $\tau$ ($T_s = n \times \tau$). Therefore, the ENC can be minimized by choosing an optimal value of the shaping time. Furthermore, as the total input capacitance increases, the contributions of both equivalent series noise sources become more significant.

**Architecture of the front-end amplifier in the ABCN-25 chip**

The design of the front-end circuitry is primarily driven by the requirement to minimize power consumption while maintaining the required noise and timing performance of the circuit. The schematic diagram of a single channel front-end amplifier and comparator, is shown in Fig. 2.5. Each channel consists of three blocks, namely the transimpedance preamplifier, the shaper providing amplification and integration, followed by the comparator stage providing the amplitude discrimination.

The preamplifier stage is built as a classical cascode stage with NMOS input transistor, nominally biased with a current of 140 µA, and an active feedback circuit employing PMOS transistor working in saturation and biased with 300 nA current. Dimensions of the input transistor, 320 µm/0.5 µm, are optimized for an input capacitance of 5 pF using the EKV MOS transistor model, as shown in Ref. [64].

The first section of the shaper consists of a two stage voltage amplifier in common source configurations, enclosed with a resistive feedback, stabilizing the gain and together with feedback capacitance C2 defining the integration time constant. The pulse gain at the output of this stage is in a range of 34 mV/fC and the peaking time is about 20 ns.

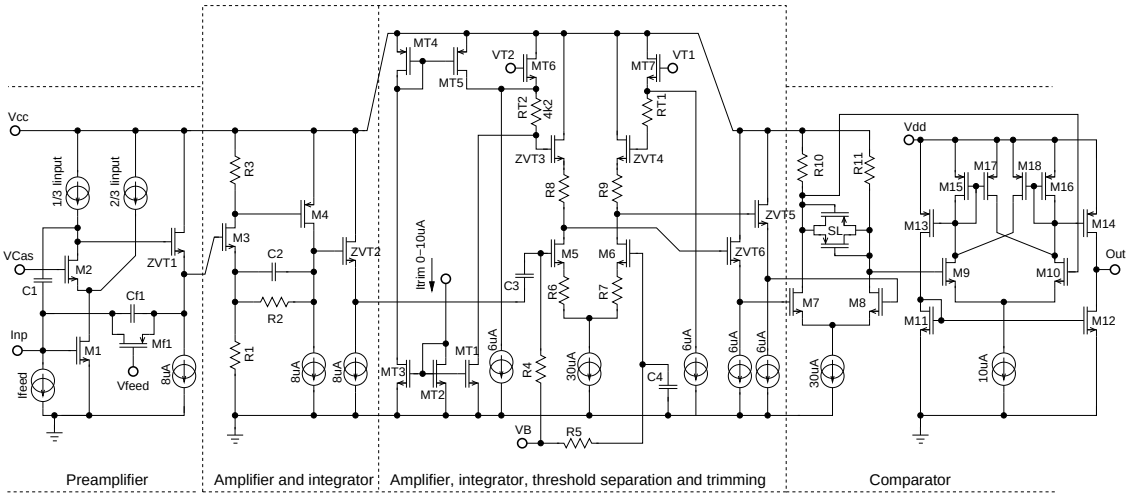



**Figure 2.5:** Schematic of the front-end.

The DC voltage at the output is controlled by the voltage Vfeed applied to the gate of the preamplifier feedback transistor and can be optimized for positive or negative input signal polarity using one of the internal biasing DAC.

The second stage of the shaper is an AC coupled differential voltage amplifier with a resistive load serving two purposes. First, it amplifies, integrates and converts the single-ended signal from the precedent section to the differential one. Furthermore, it interfaces the threshold voltage of the comparator, which is applied differentially to the gates of the NMOS source followers. The offset correction voltage is generated as a voltage drop across the load resistor according to the trimming current. The ranges of 5-bit resolution trimming DACs are programmable and can provide the trimming steps from 0.5 mV to 3 mV, which corresponds to the input signal range 0.005 to 0.03 fC, depending on the threshold offset spread.

The total gain at the differential discriminator input is 100 mV/fC and the intrinsic peaking time of the circuit is 22 ns, which ensures 25 ns peaking time including the charge collection time in the detector.

For the nominal power consumption of 0.7 mW per channel, the calculated ENC for 5 pF detector capacitance is below 800 $e^-$ RMS, allowing the use of the front-end with heavily irradiated silicon detectors. The timewalk of the comparator depends only on the amplifier peaking time and for the input charges from 1.25 to 10 fC is less than 15 ns for a threshold of 1 fC.

A more detailed description of the front-end design can be found in Refs. [57],[65] and [66].

### 2.2.3 Digital-to-analog converters

#### Principles of digital-to-analog converters

The digital-to-analog converter is a circuit that converts the digital input code to an analog output level, either a current or a voltage. In this thesis the focus is put on current-steering DAC architecture, which provides the DAC output current composed of the binary weighted ingredient currents, whose value depends on the static analog reference current and is controlled by the input binary word. The N-resolution DAC topology is presented in Fig. 2.6. It consists of a multiple current mirror M_REF, M0 ... M(N-1), built of a network of $2^{N+1}$ equally sized PMOS transistors. Transistor M_REF carries the reference current $I_{LSB}$, whereas M0, M1... M(N-1) represent the current sources, which replicates $I_{LSB}$ introducing the multiplication factor of $2^l$ in l-th branch, where l = 0, 1...N-1. N pairs of complementary switches ($S_0\overline{S_1}$... $S_{N-1}\overline{S_{N-1}}$) are controlled by N-bit input command in order to turn on the mirrored transistors in a given branch, and so the current, for a particular bit value of "1". Otherwise, if the input bit equals "0", the corresponding current source transistors in a given branch are turned off. The output current $I_{DAC}$ depends on the value of digital input word and on a reference current $I_{LSB}$ as follows:

$$I_{DAC} = I_{LSB}(2^0B_0 + 2^1B_1 + 2^1B_2 + \ldots + 2^{N-1}B_{N-1}), \tag{2.3}$$

The $I_{LSB}$ in Eq. 2.3 represents the smallest current step that can be applied to the output, the factors $2^0$–$2^{N-1}$ indicated the binary weighting of the input bits $B_0$–$B_{N-1}$, thus the $B_0$ is the Least Significant Bit (LSB) and the $B_{N-1}$ is the Most Significant Bit (MSB).

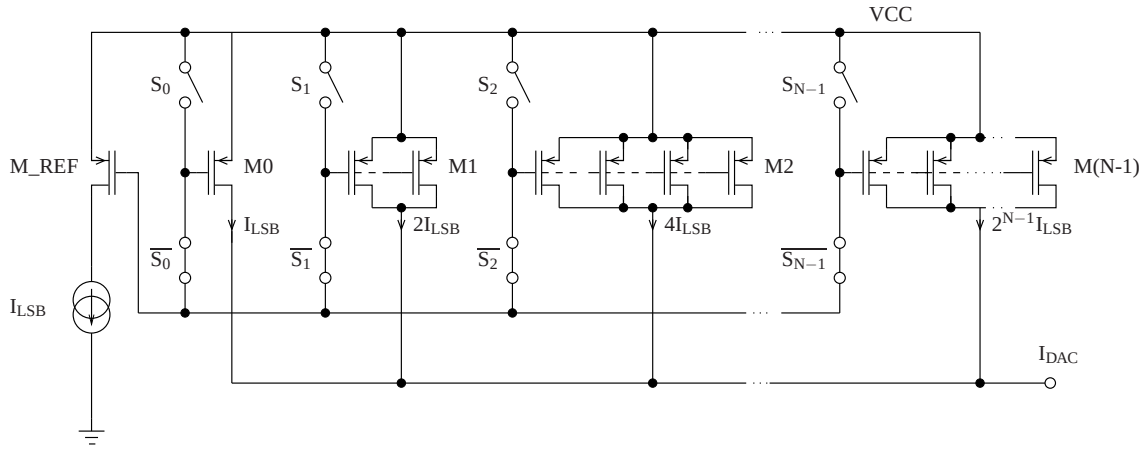



**Figure 2.6:** Typical architecture of DAC.

In the ABCN-25 chip the DACs are required to deliver the programmable DC currents, needed for proper biasing of the front-end amplifiers. However, the DAC architecture presented in Fig. 2.6 has and important disadvantage, namely the gate potential of the mirroring transistors depends on the value of input digital word (high or low state of a given bit). Keeping in mind the radiation environment, in which the DAC operates, one would observe a post-irradiation shift in the threshold voltage, which is known to be different for the MOS devices being turned on and off. This effect originates from the hole trapping in the thin oxide-transistor channel interface that shifts the transistor threshold voltage to more negative values depending on the electric field applied to the transistor gate [67]. This effect would further increase the mismatch of mirroring transistors and would result in degraded accuracy of the output current. For this reason, the typically used DAC architecture needs to be improved in order to maintain good precision in the radiation environment.

An example of enhanced N-bit DAC architecture is demonstrated in Fig. 2.7. In this

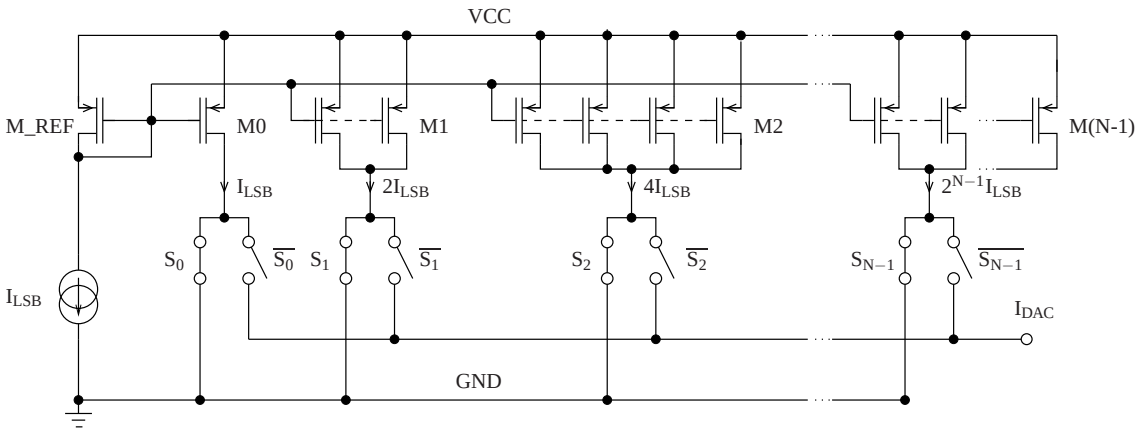



**Figure 2.7:** DAC architecture suitable for radiation environment.

topology, N branches composed of $2^N$ PMOS transistors continuously carry the scaled reference currents, which are further switched between the output nodes and the ground node, depending on the code of the input digital word. In this scheme the gate potentials of transistors M0–M(N-1) do not vary for different values of the input digital word, hence the post-irradiation shift in the threshold voltage is uniform in all transistors M_REF–M(N-1) forming the current mirror. Nevertheless, in the enhanced DAC architecture all current sources M0–M(N-1) are kept enabled, thus the power consumption has to be minimized by choosing a low reference current $I_{LSB}$.

In reality, each current source generates a current that differs slightly from the $I_{LSB}$, due to random variations of parameters of identically designed devices. Thus, the main

error the DAC suffers from is the linearity error that occurs due to the random mismatch in the conversion elements [68]. In order to ensure the monotonicity and high yield of the DAC circuitry, the statistical error analysis based on matching properties of the MOS transistor needs to be performed.

**Matching properties of the MOS transistors**

Many analog and mixed-mode circuits, such as current mirrors, differential pairs, analog to digital and digital to analog converters rely on matched devices. However, the identically designed devices, placed at small distance in the same environment and uniformly biased, they still suffer from random time-independent differences in their electrical parameters. The mismatch, that is observed between the electrical parameters of equally designed devices, is caused by two types of effect:

1. Systematic effects originating from the spread of the physical parameters, like devices dimensions, layer thickness, processing temperatures, uniformity of chemicals, which are translated into systematic electrical differences in currents and voltages. These variations occur at the level of chip-to-chip, wafer-to-wafer and batch-to-batch resulting in systematic shifts of given parameters.

2. Stochastic (random) effects caused by fluctuation of ion implantation, dopant diffusion, interface states, oxide charges, poly-Si grain effects and local mobility fluctuation. These effects results in variation of the parameters under the Gaussian distribution. The stochastic effects of mismatch cannot be avoided, however they can be minimized by following certain design techniques [69]:

   – devices are laid out equally, the best as a translated copy, keeping the same geometrical orientation, maintaining the symmetry of the elements and the interconnections, i.e. metal, contacts, surrounding;

   – elements are placed at small distance (<100 μm);

   – devices are biased identically;

   – components are kept far away from the crystal edge (>200 $\mu$m) and rest of the circuit (>40 μm);

   – extra contacts and dummy cells are placed around the sensitive cells;

   – use the common centroid layout of multiple device pairs when the temperature gradients and large distances are unavoidable [70].

Apart from these layout techniques, the statistical methods can be used to estimate the device dimensions, for which the circuit built of matched devices will exhibit a given performance with a given probability. This analysis are described below and further applied for the 8-bit DAC.

In order to predict the matching properties of the MOS transistor working in saturation, one should recall the expression, which describes the drain current in the strong inversion:

$$I_D = \frac{\beta}{2}(V_{gs} - V_{th})^2, \tag{2.4}$$

where $\beta$ equals $\mu_0 C_{OXU} W/L$, $\mu_0$ is charge-carrier effective mobility, $C_{OXU}$ is gate oxide capacitance per unit area, $W$ and $L$ are gate width and length, respectively, and $(V_{gs} - V_{th})$ is transistor overdrive voltage. Taking into account Eq. 2.4, one should identify the parameters contributing to mismatch by calculating the variance of drain current, as described by Eq.2.5:

$$\frac{\sigma^2_{\Delta I_D}}{I_D^2} = \frac{4\sigma^2_{\Delta V_{th}}}{(V_{gs} - V_{th})^2} + \frac{\sigma^2_{\Delta\beta}}{\beta^2}, \tag{2.5}$$

where $\sigma^2_{\Delta V_{th}} = A_{V_{th}}/\sqrt{WL}$ and $\sigma^2_{\Delta\beta}/\beta^2 = A_\beta/\sqrt{WL}$ are the variances of, respectively, threshold voltage $V_{th}$ and current factor $\beta$ distributions [71]. Parameter $A_{V_{th}}$ indicates the threshold voltage matching performance for a given technology. The major process parameters, which contribute to the $A_{V_{th}}$ is the dopant fluctuation in the depletion region underneath the channel and fluctuation of charge density in the gate oxide. Another technology-dependent parameter, $A_\beta$, describes the performance of the relative difference of $\beta$ for two transistors, caused by variance in gate oxide capacitance and in charge mobility. Variation of the channel length and width can usually be neglected for modern process technologies if the transistor dimensions are not minimal. The technology-dependent parameters for the IBM 0.25 µm process are specified as follows: $A_{V_{th}} = 5.9\,\text{mV}\cdot\mu\text{m}$ and $A_\beta = 2.0\,\%\cdot\mu\text{m}$ for PMOS devices and respectively $7.1\,\text{mV}\cdot\mu\text{m}$ and $A_\beta = 1.8\,\%\cdot\mu\text{m}$ for NMOS devices [72]. Following Ref. [71], the expression for minimum gate area of unit source transistor, that provides current $I_D$ with a standard deviation of $\sigma_{I_D}$ for a given technology, can be derived as follows:

$$(WL)_{min} = \frac{1}{2}\left[A_\beta^2 + \frac{4A_{V_{th}}^2}{(V_{gs} - V_{th})^2}\right] \Big/ \left(\frac{\sigma_{I_D}}{I_D}\right)^2. \tag{2.6}$$

The relative drain current standard deviation $\sigma_{I_D}/I_D$ in Eq. 2.6 should be estimated taking into account the required precision of the circuit and acceptable losses of yield due to process variations [68].

**Digital-to-analog converter linearity errors**

The quality of DAC circuits is characterized primarily by the following parameters [73]:

- Integral NonLinearity (INL) is the deviation of the actual converter data point from the point on the straight-line approximation,
- Differential NonLinearity (DNL) is the difference between each output step size of the converter and an ideal step size of 1 LSB.
- Monotonicity is an attribute of the converter, which never exhibits a decrease of the output value while the digital input is increased. Monotonic DAC behavior is ensured, if for each bit code the INL stays within range from -0.5 LSB to 0.5 LSB and the DNL is smaller than $\pm 1$ LSB.

The required INL range within -0.5 LSB to 0.5 LSB is easy to achieve for the current source steered by the LSB, since the relative current variation has to be kept below 1/2. The difficulty appears for the branches controlled by the MSB, for which the constrains for current variations has to be fulfilled by the highest current $I_{MSB}$ equal to $2^(N-1)I_{LSB}$. In this case the current accuracy described by Eq. 2.7 is requested [74]:

$$\frac{\Delta I_{MSB}}{I_{MSB}} \leq \frac{1/2LSB}{2^{N-1}LSB}. \tag{2.7}$$

Thus, the expression for maximum INL can be approximated by adding the variances of the $2^{N-1}$ current sources [74], as described by Eq. 2.8:

$$INL \approx \sqrt{2^{N-1}} \left( \frac{\sigma_{I_D}}{I_D} \right) LSB. \tag{2.8}$$

One can define the circuit yield as percentage of functional devices, which have the maximum INL less than 0.5 LSB. Following this definition, one should estimate the circuit yield as a function of relative variance of current provided by unit current source $(\sigma_{I_D}/I_D)$ for a given DAC resolution of N. Following the calculations presented in Ref. [68], the exemplary coarse yield estimation of 5-bit, 8-bit and 12-bit DACs

as a function of $(\sigma_{I_D}/I_D)$ are listed in Fig. 2.8. In following subsections the estimation of $(\sigma_{I_D}/I_D)$, for which the maximum INL less than 0.5 LSB is ensured with given yield, is applied to 8-DACs designed for the ABCN-25 chip.

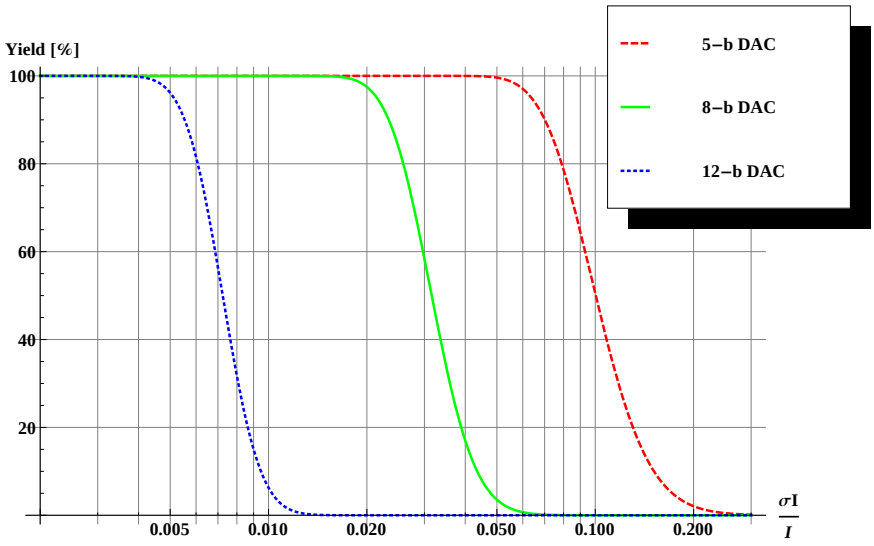



**Figure 2.8:** Yield estimation as a function of relative current standard deviation of a single current source for 5-bit, 8-bit and 12-bit DACs. Yield value describes the percentage of functional devices that have an integral nonlinearity less than 1/2 LSB.

### Digital-to-Analog Converters for ABCN-25 chip

In the ABCN-25 chips two types of DACs are used, of 5-bit and 8-bit resolution, as shown in Tab. 2.2. The sensitivity of the DAC accuracy to the radiation effects was minimized by employing the enhanced DAC architecture described above and demonstrated in Fig. 2.7. The statistical error calculations were carried for the 8-bit DACs, since the matching requirements are more demanding for converters of higher resolution. From this analysis on obtains the gate area of the unit current source transistors, which employed in the 8-bit DAC designed in 0.25 μm IBM process result in the INL<0.5LSB with 99.9% yield. Then, the obtained size of unit current source has been applied to both, 5-bit the 8-bit DACs.

The 8-bit DAC is composed of:

– 255 PMOS transistors working as the current sources formed in eight current branches,

**Table 2.2:** Specification of DACs and corresponding analog reference levels ranges, required by Front-End (FE) and calibration circuitry in the ABCN-25 chip.

| DAC Resolution | Bias currents required by FE/ to be converted to voltage required by FE | DAC Current Range [μA] | Nominal Value for FE [μA] (Multplication Factor) | Converting Resistor [kΩ] | DAC Voltage Range [mV] |
|---|---|---|---|---|---|
| 5-bit | Input transistor bias current | 30–60 | 120 (3) | – | – |
| 5-bit | Preamplifier feedback bias current | 2–10 | 0.3 (1/10) | – | – |
| 5-bit | Preamplifier buffer bias current | 6–12 | 8 (1) | – | – |
| 5-bit | Shaper bias bias current | 6–12 | 8 (1) | – | – |
| 5-bit | Shaper feedback bias current | 7–12 | 8 (1) | – | – |
| 5-bit | Differential stage bias current | 20–40 | 30 (1) | – | – |
| 5-bit | Comparator 1 bias current | 20–40 | 30 (1) | – | – |
| 5-bit | Comparator 2 bias current | 20–40 | 30 (1) | – | – |
| 8-bit | Calibration pulse | 0 - 204 | – | 1 | 0–204 |
| 8-bit | Threshold voltage positive | 0 - 204 | – | 4.2 | 0–816 |
| 8-bit | Threshold voltage negative | 0 - 204 | – | 4.2 | 0–816 |

– 8 switches (one in each current branch) controlled by the input digital word in order to switch the current in a given branch between the output node and the ground node.

The power consumption was minimized to 0.64 mW at the power supply voltage of 2.5 V, by choosing the reference current $I_{LSB}$ of 1 μA. In order to obtain circuit yield more than 99.9% for 8-bit DAC (see middle curve in Fig. 2.8), the relative current standard deviation of a unit current source $\sigma_{I_D}/I_D$ has to be below 0.012. Employing Eq. 2.6 and assuming a gate voltage overdrive ($V_{gs} - V_{th}$) of 200 mV one obtains minimum PMOS transistor area of about 14 $\mu m^2$. Adding a safety factor of 1.5 for non-ideal layout effects and a factor of

2 for degradation of matching after irradiation, one obtains a final gate area of 40 $\mu m^2$. In order to keep the gate voltage overdrive above 200 mV, the transistor width of 5 $\mu$m and length of 8 $\mu$m have been chosen.

The ranges of biasing currents and voltage reference levels requested by the front-end and calibration circuit (see Tab. 2.2) are fulfilled by multiplying the DAC output current $I_{DAC}$ by a required factor. In addition, the adequate pedestal current is introduced in order to adjust the DAC dynamic range to the desired current range specified in Tab. 2.2. As shown in Fig. 2.9, all the 5-bit DAC are followed by a current scaling network, where the current is multiplied, and then added to pedestal current $I_{OFFSET}$. In case of 8-bit threshold DACs, the pedestals can be programmed by 2-bit command. The calibration circuitry requires no current pedestals.

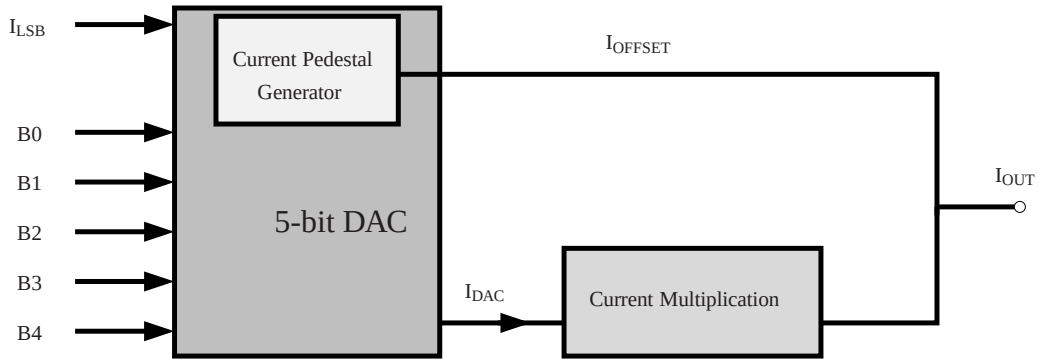



**Figure 2.9:** Block diagram of the 5-bit DAC with a current scaling network providing externally programmable bias current to the front-end part of the ABCN-25 chip.

The reference current for the DACs is generated by using the bandgap reference voltage of 1.165 V and the converting resistor $R_{CONV}$ of 60 k$\Omega$. As mentioned above, the resistance variation of low doped resistors in 250 nm CMOS process is quite high, namely 4100 $\Omega/\square$(+43/-30%) [60]. Therefore, in this design more precise polysilicon resistors were used, which provide less resistance per square area — 210 $\Omega/\square$ ($\pm$20%), hence they occupy more space on the chip. Furthermore, in this design a safety margin of -10% below and +10% above for the required current range was applied, including the variations of the converting resistor ($\pm$20%). In addition, the converting resistor was constructed from the equally sized unit cells $R_{UNIT}$, in order to minimize the total resistance sensitivity to the process variation.

In case of 8-bit DAC, the output voltage $V_{OUT}$ is generated by conversion of the DAC output current on the resistor $R_{OUT}$, as presented in Fig. 2.10. During the design process, the attention was paid to match the resistor $R_{OUT}$ with converting resistor $R_{CONV}$

in term of equal layout orientation and size of a unit-cell resistor used to construct both, $R_{OUT}$ and $R_{CONV}$ resistors. In this way, one significantly reduces the voltage-to-current conversion error due to process variations of $R_{CONV}$, by further opposite conversion, current-to-voltage, on the resistor $R_{OUT}$ matched with $R_{CONV}$. The output current and output voltage of the threshold DAC were simulated in SPICE[4], assuming the resistor variations of $\pm 20\%$. The Process-Voltage-Temperature (PVT) simulations were performed applying various sets of process corner parameters, temperature and supply voltage values, as summarized in Tab. 2.3. The comparison of simulation results is shown in Fig. 2.11. One can notice the sensitivity of the threshold current to the process variation of $R_{CONV}$. This sensitivity is compensated by reconverting the threshold current to the threshold voltage using the resistor $R_{OUT}$ matched with resistor $R_{CONV}$.

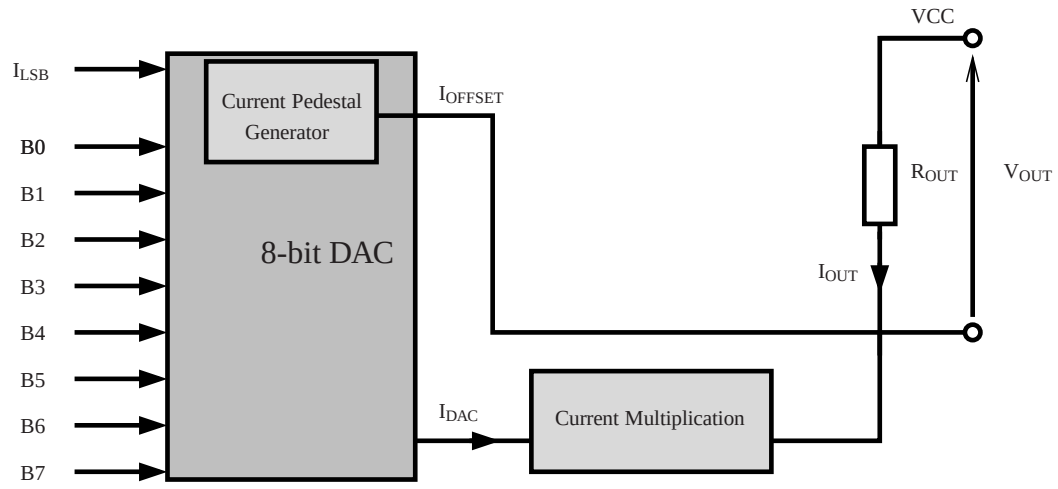



**Figure 2.10:** Block diagram of the threshold voltage generation circuit, that consists of 8-bit DAC, current scaling network and converting resistor $R_{OUT}$ providing the programmable threshold voltage $V_{OUT}$ to the comparators for amplitude discrimination in ABCN-25 chip.

Generally, the Monte Carlo simulation is a frequently used method, allowing to predict the circuit yield and sensitivity for the number of variables, which values are randomly selected according to their statistical distribution. Using the Monte Carlo simulations one can investigate how the mismatches, applied to the individual devices may accumulate and affect the circuit as a whole. These simulations can cover both kinds of manufacturing variations: random fluctuations under a Gaussian distribution and systematic errors causing a shift of given parameter distribution by a fixed amount. Unfortunately, the

[4]Simulation Program with Integrated Circuit Emphasis is an general-purpose open source simulator of the analog electronic circuits.

**Table 2.3:** Parameters used in PVT simulations. Cor1 is a nominal corner.

| Corner Name | Process Corner [σ] | Temperature [°C] | Voltage Supply [V] | Unit-cell Resistor [kΩ] (Deviation From Nominal ) |
|---|---|---|---|---|
| Cor0 | -3 | 40 | 2.2 | 9.2 (0%) |
| Cor1 | 0 | 25 | 2.2 | 9.2 (0%) |
| Cor2 | 3 | -10 | 2.0 | 9.2 (0%) |
| Cor3 | -3 | 40 | 2.2 | 7.4 (-20%) |
| Cor4 | 0 | 25 | 2.2 | 7.4 (-20%) |
| Cor5 | 3 | -10 | 2.0 | 7.4 (-20%) |
| Cor6 | -3 | 40 | 2.2 | 11.7 (+20%) |
| Cor7 | 0 | 25 | 2.2 | 11.7 (+20%) |
| Cor8 | 3 | -10 | 2.0 | 11.7 (+20%) |

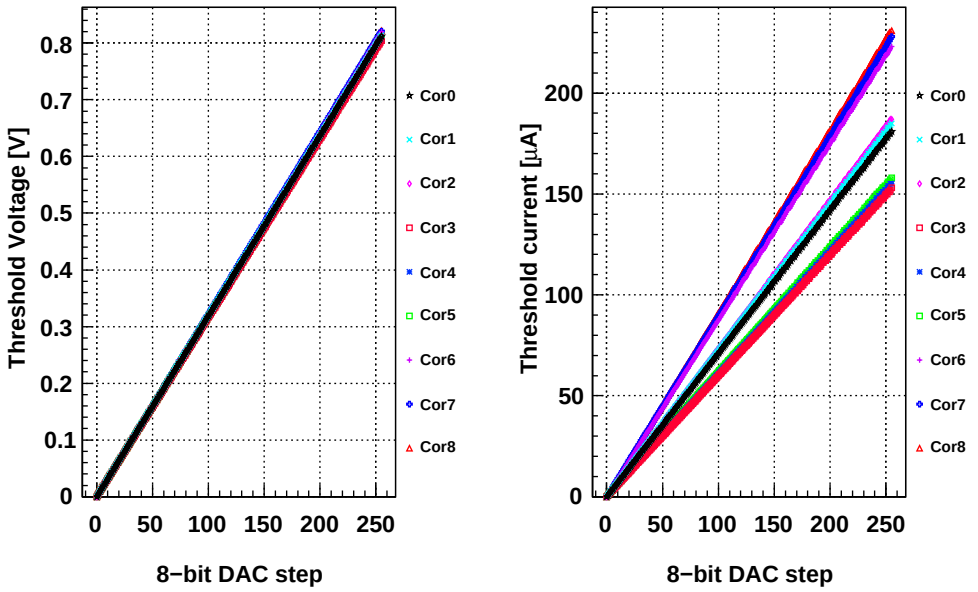



**Figure 2.11:** Threshold voltage $V_{th}$ and current $I_{th}$ as a function of digital input code. Simulation were made for process corners listed in Tab. 2.3.

Monte Carlo analysis parameters were not available in the IBM 0.25 µm process design kit. Thus, together with the process yield estimation presented above, the PVT simulations have been performed for the temperature range in which the circuit will be operated and also for the variation of the unit resistor value calculated for the batch-to-batch mismatch.

The PVT simulation results have been used to evaluate the INL of the threshold voltage generation circuit for different corner parameters, as presented in Fig. 2.12. One

can notice a very low INL with maximum value of -0.14 LSB for maximum resistor variation providing both resistors are matched.

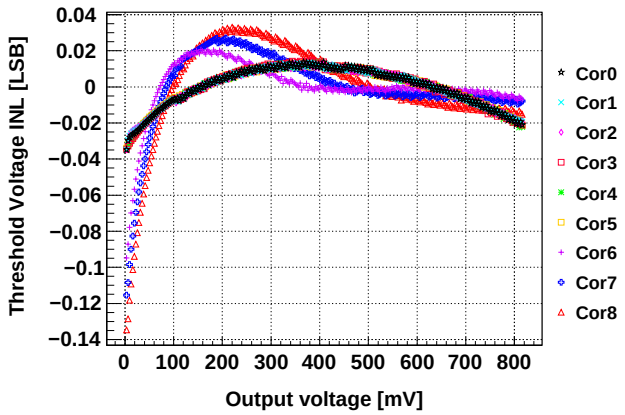



**Figure 2.12:** Integral nonlinearity of the simulated threshold voltage. Simulation were made for process corners listed in Tab. 2.3.

### Calibration circuit

Each of the 128 readout channels comprises an internal capacitor of 50 fF connected to its input for calibration purposes. The capacitors are charged by the voltage steps delivered by four internal calibration lines, each line is connected to every fourth front-end channel. The address of the calibration line, the amplitude of the calibration voltage step signal and its delay are set via the control logic. The calibration signal is characterized in Tab. 2.4

**Table 2.4:** Performance of the calibration pulse.

| Property | Description |
|---|---|
| Amplitude range | 0–204 mV (equivalent charge range of 0 – 10.2 fC) |
| Amplitude step | 0.8 mV (equal to a charge step of 0.04 fC) |
| Absolute accuracy of amplitude | 5% over full process skew |

The schematic diagram of the calibration circuit is presented on Fig. 2.13. The 8-bit DAC output current $I_{DAC}$ is mirrored to four calibration lines with a multiplication factor of 0.8. The generated currents $I_{cal0} - I_{cal3}$ are switched between the calibration output nodes $V_{cal0} - V_{cal3}$ and the ground by switches S0 – S3, which are controlled by a command that turns each calibration line on and off. While a given calibration line is turned on, the output current flows across the 1 kΩ converting resistors $R_{CAL}$, generating

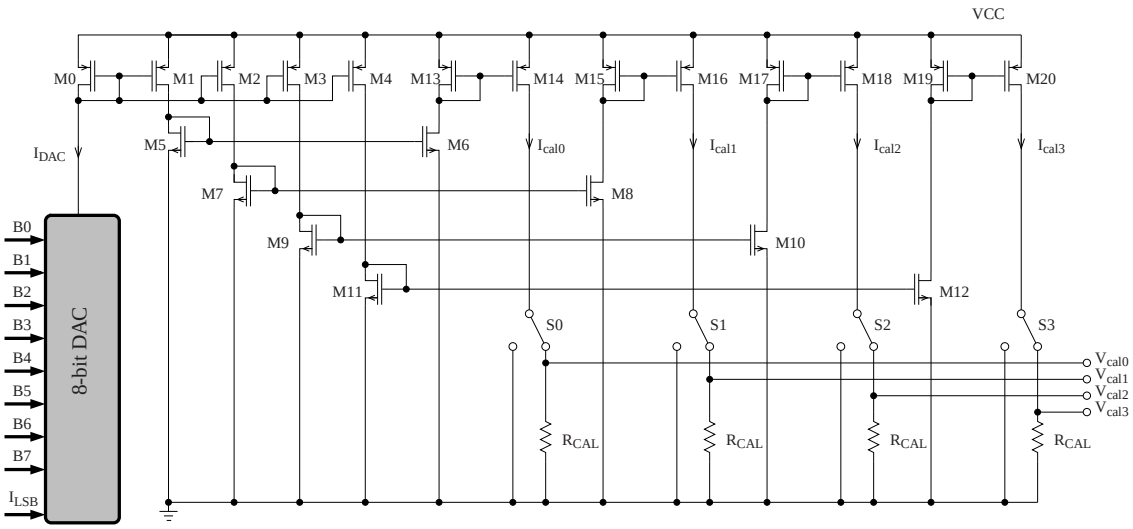



**Figure 2.13:** Schematic diagram of the calibration circuit designed for ABCN-25 chip.

the calibration voltage step. This resistor is also matched to the resistor $R_{CONV}$ in order to reduce the sensitivity of the calibration output voltage to process variation of the resistor.

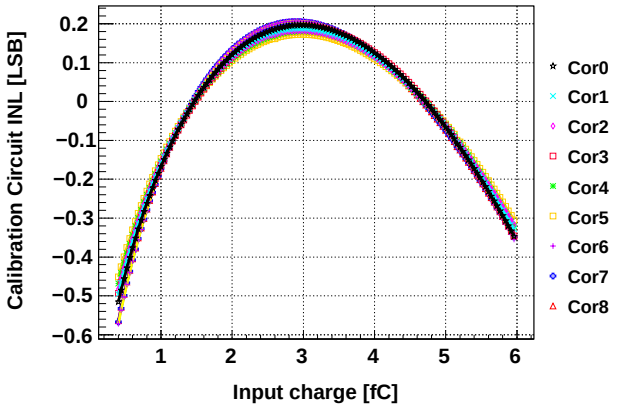



**Figure 2.14:** Integral nonlinearity of the calibration circuit output voltage. Simulation were made for process corners listed in Tab. 2.3.

The calibration circuitry was simulated in SPICE for various process corners (see Tab. 2.3) in order to estimate the INL. The results, presented in Fig. 2.14, show the maximum INL of -0.58 LSB for the input charge range from 0.4 to 6 fC, what slightly exceeds the required range of $\pm 0.5$ LSB for three lowest values of input charge.

## 2.3 Test results of the ABCN-25 chip

The ABCN-25 design has been fabricated and its full functionality has been demonstrated in initial evaluation tests. The performance of the chip has been measured with respect to both, analog and digital functions, by using a dedicated test system. In this thesis the focus is put on the analog part of the chip, namely noise performance of the front-end circuitry and functionality of the calibration circuit and DACs after irradiation, as described in following subsections. The detailed description of the measurement results can be found in Ref. [66].

### 2.3.1 Noise performance of the front-end circuitry

The noise figures of the front-end have been measured for chips mounted on a dedicated board, with a specific "clean" layout in front of the channel input pads, to minimize parasitic capacitances of tracks and to reduce crosstalk from the digital signals or power supply lines. Small Surface Mount Device (SMD) type capacitors can be added the two channels inputs to perform the measurement of the noise versus the input capacitance. The typical measurement results are summarized in Fig. 2.15. For short strips the expected strip capacitance should not exceed 5 pF including parasitic capacitance of bonding pads and bonding wires. The measurements were made for external capacitance from 0 pF to 6.5 pF, to which a parasitic value of 0.5 pF was added, due to stray capacitances of the printed circuit board. The measurement at 5.5 pF (5 pF of external capacitor) shows the ENC below 800 e- at nominal input transistor bias current $I_D$ of 140 μA. This value agrees quite well with the estimated noise value, represented by the middle curve in the Fig. 2.15.

### 2.3.2 Performance of the calibration circuitry and the digital-to-analog converters

The calibration circuitry and DACs were characterized with respect to its linearity performance before and after irradiation. Two samples of ABCN-25 chip were irradiated up to 100 Mrad and tested. Sample 1 was measured before irradiation, after 100 Mrad irradiation and after three months annealing at room temperature. Sample 2 was measured after 75 Mrad then irradiated up to 100 Mrad and tested after annealing (three months at room temperature). The comparison of results, obtained for both samples measured after

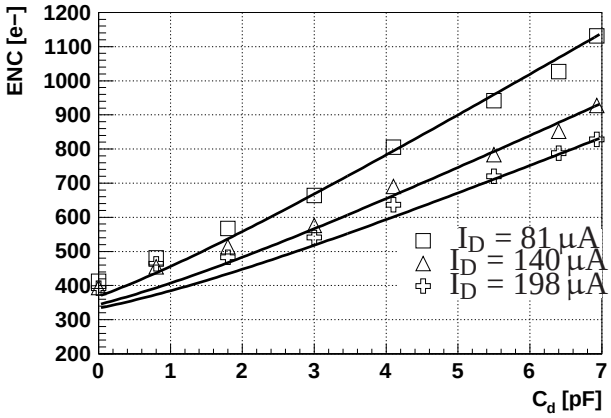



**Figure 2.15:** Estimated (solid line) and measured (marks) noise averaged from two front-end channels of ABCN-25 for different values of the detector capacitance.

annealing, as well as the behavior of Sample 1 before irradiation, after irradiation and after annealing, are presented below.

1. Calibration circuit.

   Fig. 2.16 shows the results obtained by taking into account the charge range from 0.4 to 6 fC (bit steps: 10–150). One can conclude, that during the irradiation process, the gain of the calibration circuit (the slopes in Fig. 2.16b) varies. The measurement of the pre-irradiated Sample 1 (see Fig. 2.16d) shows the maximum INL of 0.4 LSB. The INL value increases after the irradiation to 0.55 LSB and further increases to 0.8 LSB after annealing. The maximum DNL reaches 0.1 LSB 0.3 LSB and 0.8 LSB, respectively for the pre-irradiated, irradiated and annealed Sample 1 (see Fig. 2.16f). The comparison of transfer characteristics measured for two annealed samples (Sample 1 and Sample 2), presented in Fig. 2.16a, shows about 20% variation in the slope value. The comparison of INL, shown in Fig. 2.16c, indicates better linearity performance of calibration circuit after annealing for Sample 2 (0.55 LSB) in comparison to Sample 1 (0.8 LSB). Similarly the DNL is lower for the annealed Sample 2 (reaching the level of 0.6 LSB) than for Sample 1 (0.8 LSB) as shown in Fig. 2.16e.

2. Threshold positive DAC.

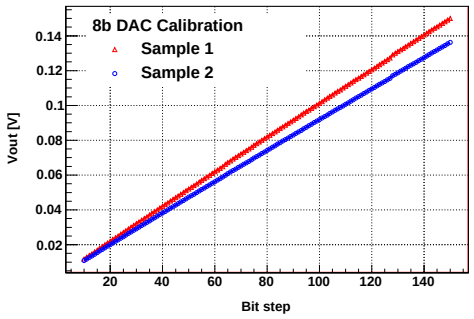
   The results are presented in Fig. 2.17. The transfer characteristic after irradiation changes about 10%, in comparison to pre-irradiated one (see Fig. 2.17b). The INL

for Sample 1 rises from 0.22 LSB (pre-irradiated) to 1 LSB (after irradiation), and decreases to 0.62 LSB (after annealing), as shown in Fig. 2.17d. Respectively, the DNL changes as follows (Fig. 2.17f): 0.3 LSB, 0.6 LSB and 0.9 LSB. Comparison of annealed Sample 1 and Sample 2 shows, respectively, the maximum INL of 0.5 LSB and 0.8 LSB (Fig. 2.17c) and maximum DNL of 0.5 LSB and 0.9 LSB (Fig. 2.17e).

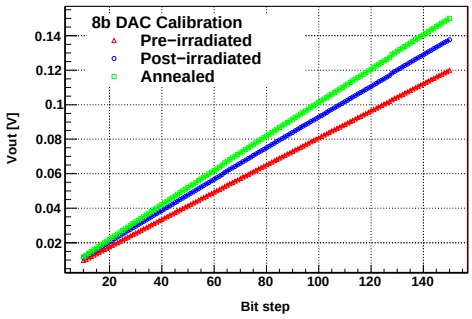
3. Threshold negative DAC.

   The results are presented in Fig. 2.18. The threshold negative DAC exhibits about 10% change in gain when comparing the measurements performed before and after irradiation (Fig. 2.18b). The evolution of maximum INL for the non-irradiated, irradiated and annealed Sample 1 has been found as follows: 0.24 LSB, 0.5 LSB and 0.5 LSB (Fig. 2.18d), whereas DNL: 0.2 LSB, 0.5 LSB and 0.3 LSB (Fig. 2.18f). Annealed Sample 2 shows slightly better linearity performance in comparison to annealed Sample 1, the maximum INL of 0.28 LSB (Fig. 2.18c) and DNL of 0.15 LSB were found (Fig. 2.18e).

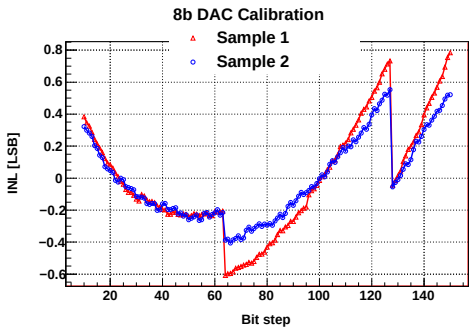
The functionality of DACs after the irradiation up to 100 Mrad has been proven, however a decrease in DACs precision due to radiation damage is observed. One can conclude that an implementation of layout techniques enhancing the radiation-resistance of the circuitry do not ensure high accuracy of the matched electronic devices after irradiation. Therefore, it is recommended to design precise components, like DACs, with an additional safety margin in critical parameters, which allows for degradation of performance after irradiation. In the particular case of DACs, one can consider increasing the resolution by adding one additional bit. This solution will however cost much higher power consumption, since each additional bit doubles the amount of current carried in the device.



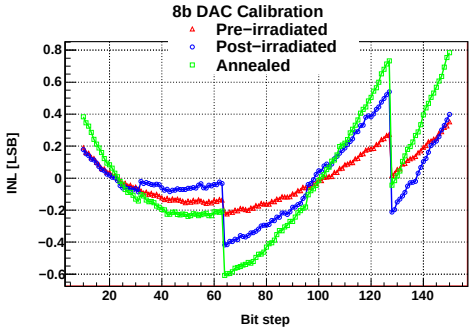

**(a)** Transfer characteristics, after annealing.



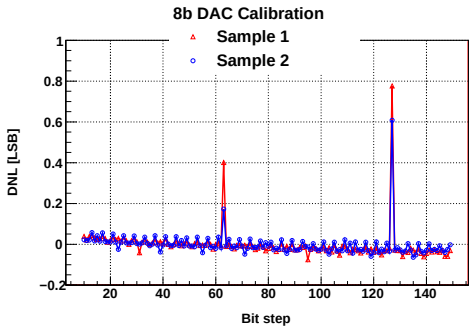

**(b)** Transfer characteristics, Sample 1.



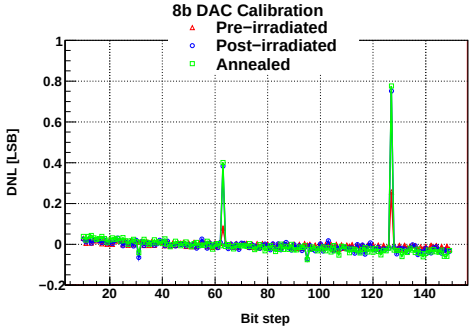

**(c)** INL, after annealing.




**(d)** INL, Sample 1.

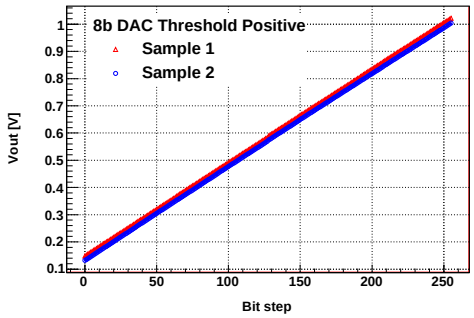



**(e)** DNL, after annealing.

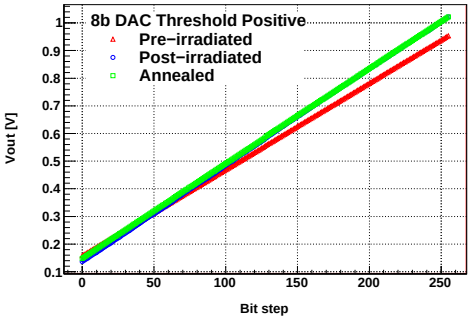



**(f)** DNL, Sample 1.

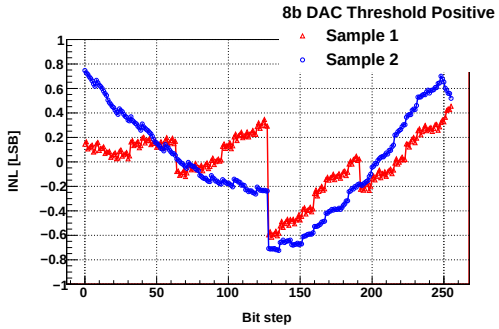
**Figure 2.16:** Parameters of the calibration circuit before and after irradiation. The comparison of two samples, irradiated and measured after annealing at room temperature, are shown in (a), (c) and (e). Sample 1 was measured before and after the irradiation, as well as after 3 months of annealing at room temperature; comparison of the results is shown in (b), (d) and (f).



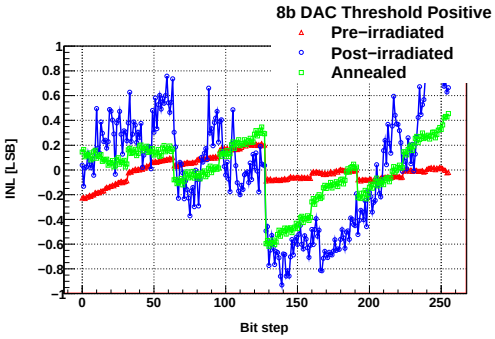

**(a)** Transfer characteristics, after annealing



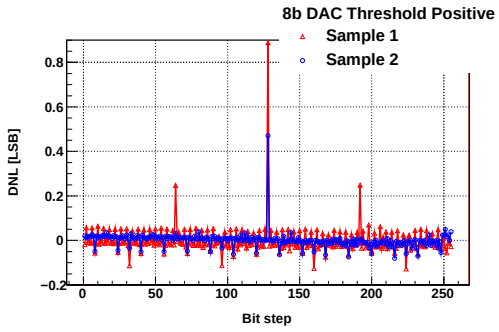

**(b)** Transfer characteristics, Sample 1



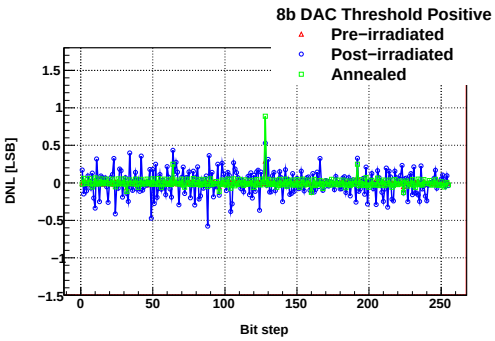

**(c)** INL, after annealing




**(d)** INL, Sample 1

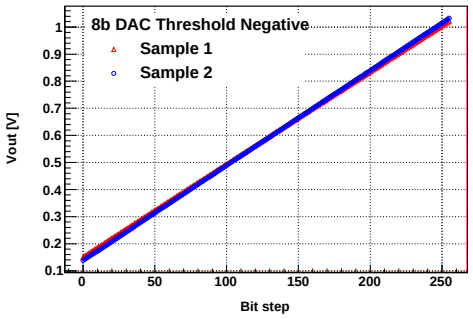



**(e)** DNL, after annealing

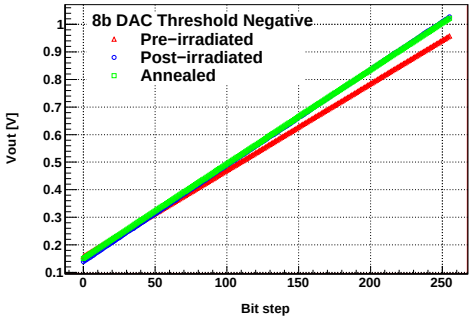



**(f)** DNL, Sample 1

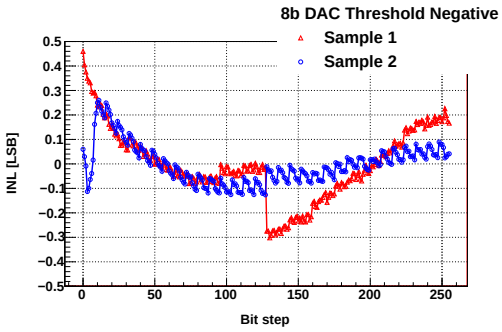
**Figure 2.17:** Parameters of the threshold positive DAC before and after irradiation. The comparison of two samples, irradiated and measured after annealing at room temperature, are shown in (a), (c) and (e). Sample 1 was measured before and after the irradiation, as well as after 3 months of annealing at room temperature; comparison of the results is shown in (b), (d) and (f)



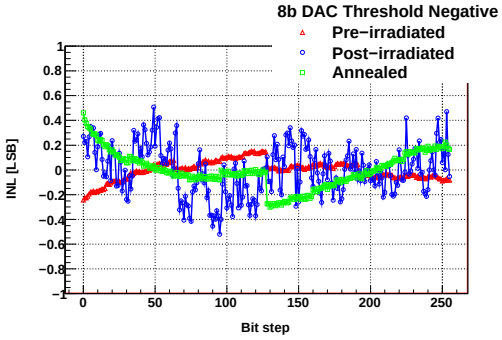

**(a)** Transfer characteristics, after annealing



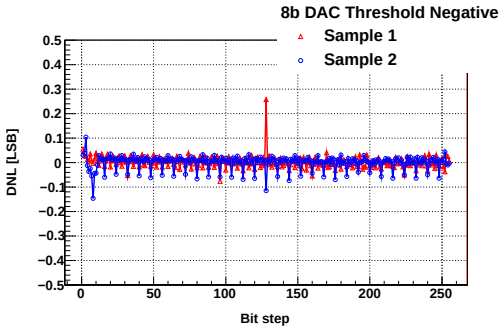

**(b)** Transfer characteristics, Sample 1



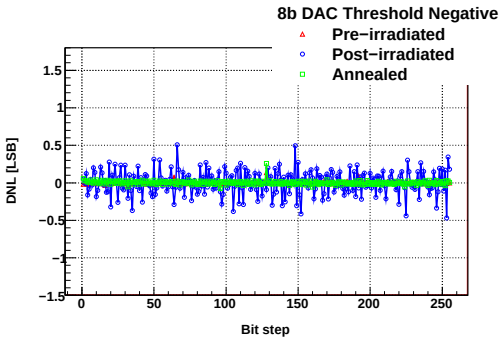

**(c)** INL, after annealing




**(d)** INL, Sample 1




**(e)** DNL, after annealing




**(f)** DNL, Sample 1

**Figure 2.18:** Parameters of the threshold negative DAC before and after irradiation. The comparison of two samples, irradiated and measured after annealing at room temperature, are shown in (a), (c) and (e). Sample 1 was measured before and after the irradiation, as well as after 3 months of annealing at room temperature; comparison of the results is shown in (b), (d) and (f)

## 2.4 Conclusion on the ABCN-25 development

The ABCN-25 chip has been designed and manufactured in IBM CMOS 0.25 μm technology. It provides all functions required for processing the signals from 128 strips of a silicon strip detector in the ATLAS Inner Detector upgrade, employing the binary readout architecture. The ABCN-25 chip is an intermediate step towards the implementation of this readout architecture in a more advanced process for the final design, optimized for both — short and long silicon strip detectors. The developed ASIC serves as a test vehicle for the silicon strip sensor R&D program, as reported in Refs. [75] and [13]. The analog parameters of the front-end channel measured on the prototype chip samples follow the specification listed in Ref. [57]. The estimation of noise behavior of the front-end channel agrees quite well with the measurement results. In the next step, the design of the same functionality will be transferred to the 130 nm technology, aiming at lowering the power dissipation. The irradiation tests of the ABCN-25 chip exhibit an noticeable decrease in accuracy of precise circuits based on matched devices — the calibration circuit and digital-to-analog converters. Thus, it is recommended to further improve the accuracy of critical devices, in order to ensure their proper and precise functionality in a high radiation environment.

# Chapter 3

# Thin Film on ASIC technology for CLIC experiment

Relatively low event rate and low radiation level of the CLIC experimental environment compared to the S-LHC would make the currently available pixel sensor technologies suitable for the vertexing purposes. However, CLIC aims at very precise measurements, thus its main challenges come from minimizing the material budget and power dissipation in a large number of readout channels connected to greatly segmented pixel detectors. For these reasons, strong constraints are imposed on detector thickness, amount of electronics material, number of power cables, mechanical support structures and cooling system.

The beam time structure poses two additional subjects to be investigated from the vertex detector design point of view:

1. A low duty cycle of CLIC puts forward a concept of pulsed powering of the detector system in order to decrease the average power consumption. Since a train repetition rate of 50 Hz is foreseen for the CLIC beam, the power supply of sensors could be switched off between collisions. Though, no realistic scheme for pulsed powering system has been proposed so far.

2. A single train comprises 312 bunches with a time separation of 500 ps. In order to identify and separate the secondary vertices, one has to associate them with a given bunch by measuring the time stamp of vertices. An ideal solution would be to associate time and spatial measurements in all pixel layers of the vertex detector. However, implementing the fast time stamp measurement in each readout ASIC increases considerably power consumption of the front-end electronics. Another

concept being investigated assumes special layers that would provide time stamping in the vertex region. However, such layers would still cause a severe impact on the material budget.

In parallel to Monolithic Active Pixel and Hybrid Pixel technologies, new ideas aiming at improving detector performance are being developed [76],[77] in order to fulfill the requirements posed by CLIC. One of these alternatives, called Thin Film on ASIC technology, combines the advantages of both technologies mentioned above. The TFA structure consists of a thin film sensor deposited directly on top of an ASIC. A low deposition temperature of the sensor material, around 200 °C, is compatible with post-processing of standard CMOS wafers. This allows for separate design and optimization of the sensor and the readout electronics, similarly to Hybrid Pixel detectors technology. The research, which has been made on TFA technology based on hydrogenated amorphous silicon (a-Si:H) sensors, as described in this thesis, has aimed at providing a proof of principle of this concept. The TFA structure is briefly described in Section 3.1. Section 3.2 and Section 3.3 describe the sensor properties and the front-end electronic architecture, respectively. The noise estimation of the designed front-end electronics is presented in Section 3.4. The experimental results are shown in Section 3.5, the development of the AFRP chip is concluded in Section 3.6.

## 3.1 Thin Film on ASIC technology

Thin Film on ASIC is a novel solid state detector technology based on direct deposition of a thin sensor layer on top of an post-processed ASIC. A schematic diagram of the TFA structure is presented in Fig. 3.1. The bottom part of TFA structure is a post-processed ASIC, containing number of readout channels — front-end preamplifiers — whose inputs are connected to the pixelized top metal electrodes. This pixelized ASIC top metal, which serves also as a sensor bottom contacts (anodes), defines the sensor segmentation. The sensor is built on top of the ASIC by consecutive depositions of *n*-doped, intrinsic and *p*-doped films of a-Si:H forming a *p*-*i*-*n* diode. In order to keep sensor segmentation without patterning, its bottom *n*-layer, which is common over all the ASIC surface, is made of a low conductivity material, providing an isolation between neighboring pixels higher than 10 MΩ. The sensor common top electrode (cathode), deposited on top of *p*-layer of the sensor, is implemented as a Transparent Conductive Oxide (TCO) made of Indium Tin Oxide. The sensing layer, placed between the ASIC top metal and the TCO electrode, is made of hydrogenated amorphous silicon (a-Si:H),

detailed in Section 3.2. The direct deposition approach, applied in the TFA structure, enables small pixel size, since no limitation is imposed by bump bonding, nor wire bonding.

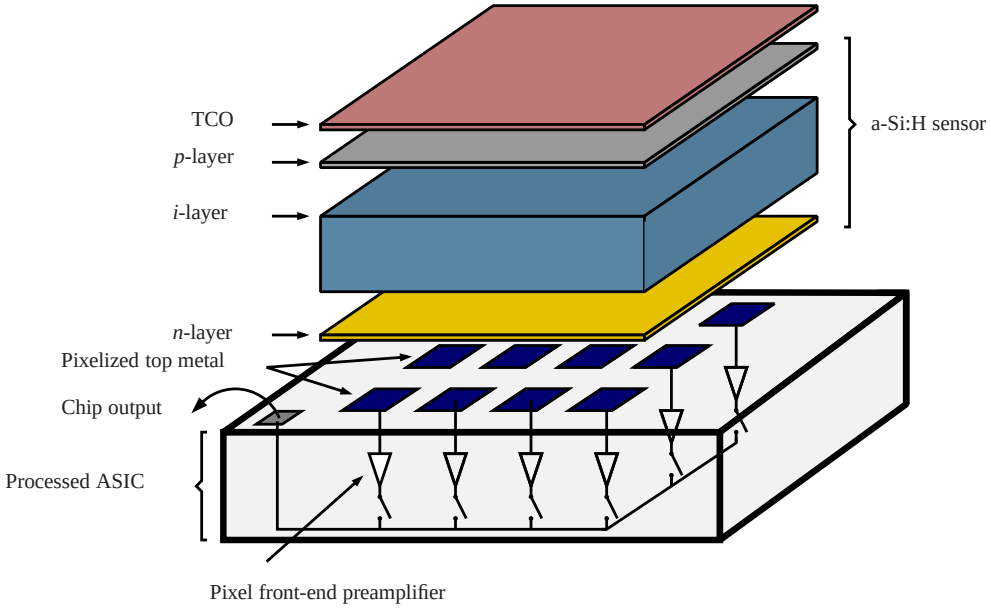



**Figure 3.1:** Schematic representation of the TFA structure, composed of a *p-i-n* diode deposited directly on an ASIC.

## 3.2 Sensor

The a-Si:H material has been studied over the past 30 years and is widely used in solar cells industry and in various imaging devices [78]. Amorphous silicon is a non-crystalline form of silicon, which is a four-fold coordinated atom, tetrahedrally bonded to four neighboring silicon atoms. In the amorphous silicon, the long-distance order of the periodic structure is not present, contrary to the crystalline silicon. Even if a-Si atoms do not form a continuous crystalline lattice, they still hold a short-distance order with the nearest neighbors. However, some of the a-Si atoms do not bond to four neighbors, presenting dandling bonds. These dandling bonds are defects in the lattice, which result in anomalous electrical behavior. In order to reduce the dangling bonds density by several orders of magnitude, a-Si can be passivated by hydrogen, forming the hydrogenated amorphous silicon (a-Si:H). An attractive feature of the a-Si:H sensors is a high radiation hardness [79], which makes this material an interesting and promising option for tracking detectors in high-energy physics experiments. Though recent results show that more

studies need to be done on this material to conclude on its potential higher radiation hardness compared to crystalline silicon [78]. More detailed study of a-Si:H sensors can be found in Ref. [80].

Despite significant progress in technology of depositing thin film hydrogenated amorphous silicon on ASICs, the signal charges delivered by such sensors are small, about 37 $e^-/\mu m$ for a Minimum Ionizing Particle (MIP) [81] compared to around 72 $e^-/\mu m$ [25]. Taking into account achievable diode thicknesses of 15 $\mu m$, which can be fully depleted, one can expect signals up to 600 $e^-$. Therefore, a low noise and high gain front-end circuit is of primary importance.

## 3.3 Front-end electronics

A schematic diagram of the developed front-end circuit is shown in Fig. 3.2. The circuit is based on a charge sensitive preamplifier built around an unbuffered cascode stage with feedback capacitor $C_f$ of 1.3 fF, which provides a sufficiently high gain of 800 mV/fC in the single stage amplifier.

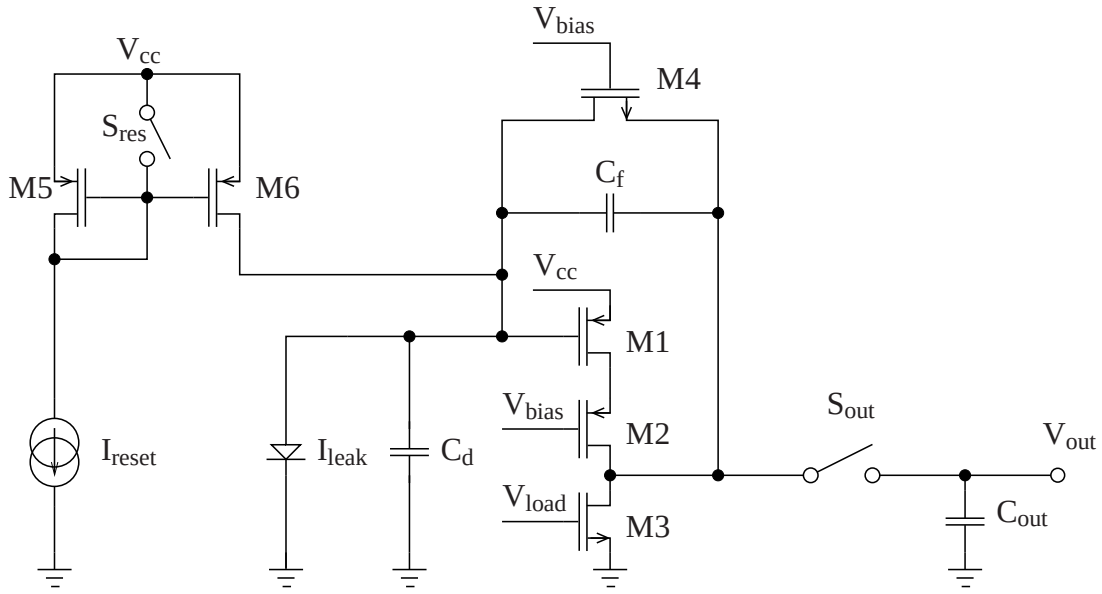



**Figure 3.2:** Schematic diagram of the charge sensitive preamplifier with the pulsed reset.

The active feedback architecture is implemented, employing the pulsed reset scheme for discharging the feedback capacitor (see Section 2.2.2). The dimensions of the input PMOS transistor M1 are 6 $\mu m$/0.28 $\mu m$, which allows to keep the intrinsic gate capacitance of transistor M1 small, about 10 fF. This capacitance and the detector

capacitance $C_d$ compose the total input capacitance $C_{int}$ of about 40 fF, which determines the noise performance of the circuit.

The preamplifier works as a gated integrator with acquisition time $t_{acq}$ and integration time constant $\tau_i$. The operation sequence starts with the reset phase, when switch $S_{res}$ is open, and the reset current $I_{reset}$ flows through PMOS current mirror M5–M6 feeding the NMOS transistor M4. The reset current is set low enough, to ensure that M4 is operating in weak inversion. The gate of this transistor is biased by constant voltage $V_{bias}$, causing continuous discharging of the feedback capacitor $C_f$ while the reset current is provided. During the reset phase, the switch $S_{out}$ stays open and no incoming signals are sent to the preamplifier output. In the next step, the preamplifier operates in acquisition mode, when the input signals are amplified and stored in the preamplifier output. In this phase, switch $S_{res}$ is closed, and no reset current is provided to transistor M4 in the feedback loop. The input signal is integrated on the feedback capacitor $C_f$ and transferred through switch $S_{out}$ to the output, charging the capacitor $C_{out}$. In the third operation phase, switch $S_{out}$ opens and the output voltage level $V_{out}$ from the pixels are sent out off the chip. While the 4096 output voltages $V_{out}$ are read out through a serial multiplexer, the preamplifier is kept in the reset mode.

During the reset phase, the feedback capacitance is discharged through the transistor biased with a constant current. This is a novel solution compared to commonly used voltage-controlled ($V_{bias}$-controlled) reset transistor. This new schema has been investigated because the parasitic charge injection from the reset signal to the very small feedback capacitor $C_f$ would lead to saturation of the preamplifier.

## 3.4 Noise estimation

The design presented above was optimized for the linear collider application, where the time window when interesting events may appear is short, in a range of hundreds nanoseconds. In order to minimize the influence of the sensor leakage current on the readout electronics, the preamplifier should be switched to the acquisition mode, which provides high gain, only when interesting events arrive to the sensor. During this time period, the noise of the front-end electronics needs to be minimized to ensure high signal to noise ratio. The noise estimation is performed separately for the reset phase and for the acquisition phase in the frequency domain. Since this circuit is time-variant and its input-to-output transfer function depends on the actual mode of the preamplifier operation,

the noise calculations are more complex than in the case of time-invariant circuits. It is assumed that the SNR in the acquisition phase is determined by two noise components:

1. Noise generated in the preamplifier during the acquisition phase,

2. Noise generated in the preamplifier during the reset phase , which stays “frozen” in the preamplifier when it is switched from reset to acquisition phase.

The first term is due to noise originating from the cascode input and load transistors (M1 and M3), as well as from the sensor leakage current. In order to describe the second term, the following model is assumed: when the preamplifier operates in the reset mode, the noise at the output node is fed back to the input node through the feedback loop. When the preamplifier is switched from the reset to the acquisition mode, the noise at the input node is sampled. In other words, instantaneous value of noise is “frozen” in the input node, introducing the additional noise component. In the acquisition phase this noise component is amplified and shaped by the acquisition phase transfer function.

The noise calculations have been performed by using the noise power spectra densities proposed by van der Ziel [82] and the EKV analytical MOS transistor model [83]. See Appendix A for more details on EKV model. The noise sources of MOS transistor are summarized in Appendix B. The description of noise analysis of the preamplifier used in AFRP chip is presented in Appendix C.

### 3.4.1 Noise related to the preamplifier operating in the acquisition mode

The main noise sources, which are present in the preamplifier operating in the acquisition mode, originate from the cascode input transistor M1, cascode load transistor M3 and from the detector leakage current.

In this analysis it is assumed that the overall shaping function of the preamplifier is equivalent to a gated integrator. The integration time constant $\tau_i$ is defined by the bandwidth of the unbuffered cascode stage loaded with input, output and feedback capacitances. In addition, a finite readout time $t_{acq}$ cuts off the low frequency noise components. This phenomena is approximated by a transfer function of a high-pass filter characterized by a time constant equal to acquisition time $t_{acq}$. A detailed analysis of the preamplifier, shown in Appendix C, leads to the expressions describing the frequency transfer functions of the preamplifier for the parallel and series noise components —

Eqs. C.9 and C.15 respectively. These transfer functions are further used to calculate the RMS noise values at the preamplifier output as described by Eqs. C.34–C.39.

Assuming that the acquisition time $t_{\mathrm{acq}}$ is much longer than the integration time constant $\tau_{\mathrm{i}}$, the charge gain of the circuit is calculated as the reciprocal the feedback capacitance $C_f$, as defined by Eq. C.27. By combining the expressions for circuit gain and the RMS noise values at the preamplifier output, as described by Eq. C.26, one finds following ENC formulas:

1. Noise related to the input transistor M1.

   (a) Channel thermal noise:

$$\mathrm{ENC}_{\mathrm{THM1}} = \frac{\sqrt{2}C_f}{q}\sqrt{\frac{\kappa^2 knTt_{acq}\gamma}{\lambda^2 g_{m1}\pi + \lambda g_{m1}t_{acq}}}, \tag{3.1}$$

   where

$$\kappa = \xi/\eta, \tag{3.2}$$

$$\lambda = \zeta/\eta, \tag{3.3}$$

$$\eta = C_{int}g_{ds3acq} + C_f(g_{ds3acq} + g_{m1}), \tag{3.4}$$

$$\zeta = 2(C_{int}C_{out} + C_f(C_{int} + C_{out})), \tag{3.5}$$

$$\xi = (C_f + C_{int})g_{m1}, \tag{3.6}$$

   $g_{m1}$ is a transconductance of the input transistor modeled using the EKV MOS transistor model as defined in Eq. A.4 , $C_{int}$ and $C_{out}$ are the total input and output capacitances, $\gamma$ is a EKV model parameter defined by Eq. B.8, $g_{ds3acq}$ is an output conductance of transistor M3 operating in the acquisition phase. The remaining parameters of this and following ENC expressions are listed in Tab. A.1. The values of preamplifier parameters taken from SPICE simulations and used further in the noise analysis are detailed in Tab. C.1.

   (b) Gate induced current (GIC) noise:

$$\mathrm{ENC}_{\mathrm{GICM1}} = \\ = \frac{4C_fC_{OX}}{3\sqrt{5}q}\sqrt{\frac{kTt_{acq}\left(2\eta C_f^2(2\pi\tau_b + t_{acq}) + \zeta\left(2C_f^2\pi + g_{m1}^2\tau_b t_{acq}\right)\right)\gamma}{\zeta g_{m1}n\tau_b(\zeta + 2\eta\tau_b)(2\pi\tau_b + t_{acq})(\zeta\pi + \eta t_{acq})}}, \tag{3.7}$$

where $C_{OX} = C_{OXU}LW$, $C_{OXU}$ is Gate-to-Source capacitance per unit area, $W$ and $L$ are width and length of input transistor gate, and $\tau_b$ is an additional integration time constant of the buffer stages in the pixel matrix readout circuit. The $\tau_b$ was introduced to the calculations as shown in Eq. C.34 and according to simulations made in SPICE $\tau_b$ equals 5 ns.

(c) Flicker noise,

$$\mathrm{ENC_{FM1}} = \frac{C_f}{q}\sqrt{\frac{\kappa^2 K_a t_{acq}^2 \mathrm{Log}\left[\frac{\lambda\pi}{t_{acq}}\right]}{C_{OXU}^2 LW\left(\lambda^2\pi^2 - t_{acq}^2\right)}}, \tag{3.8}$$

where $K_a$ as a flicker noise coefficient.

(d) Correlation term of the GIC and channel thermal noise represented in a frequency domain.

$$\mathrm{ENC_{CorrM1}} = \\ = \frac{2C_f}{q}\sqrt{\frac{2C_{OX}\kappa kT\gamma\left(C_f(\zeta+\eta\lambda)+\lambda(2\eta C_f+\zeta g_{m1})\mathrm{Log}\left[\frac{\eta\lambda}{\zeta}\right]\right)}{3\pi\zeta\lambda(\zeta+\eta\lambda)g_{m1}}}. \tag{3.9}$$

Fig. 3.3 shows the ENC related to transistor M1 as a function of the input transistor bias current $I_D$ calculated for the acquisition time $t_{acq}$ of 1 µs. The total ENC

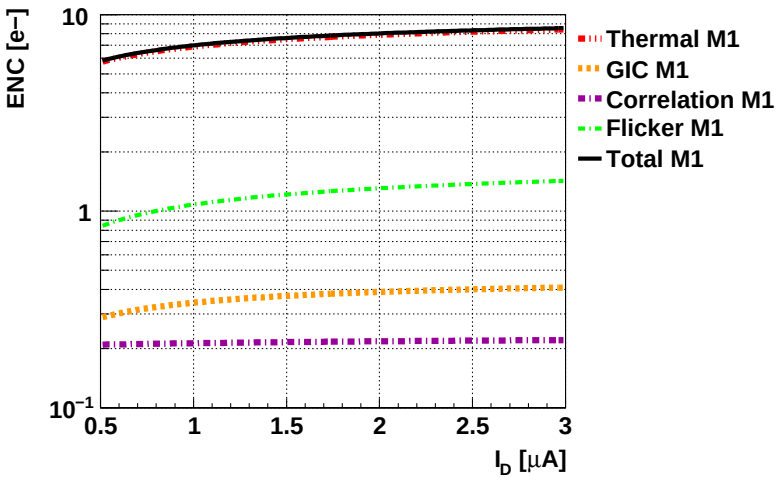



**Figure 3.3:** Calculated noise originating from the input transistor in the acquisition phase for $t_{acq}$ of 1 µs.

has been calculated as a square root of sum of squared ENC terms defined by Eqs. 3.1,3.7–3.9. One can notice that the channel thermal noise dominates over the other noise terms. The calculated total noise of the input transistor M1 is below 10 e- over the bias current range from 0.5 µA to 3 µA.

2. Channel thermal noise of the cascode load transistor M3.

   The ENC value of channel thermal noise of transistor M3 has been calculated using Eqs. C.26 and C.37:

$$\mathrm{ENC_{THM3}} = \frac{\sqrt{2}C_f}{q}\sqrt{\frac{\kappa^2 knT t_{acq}\gamma g_{m3}}{\lambda^2 g_{m1}^2\pi + \lambda g_{m1}^2 t_{acq}}} \tag{3.10}$$

3. The shot noise originating from the a-Si:H sensor leakage current.

   The ENC related to the detector leakage current has been calculated employing Eqs. C.26 and C.35:

$$\mathrm{ENC_p} = \frac{C_f}{q}\sqrt{\frac{4\eta C_f^2 I_{leak}\pi q t_{acq} + \zeta g_{m1}^2 I_{leak} q t_{acq}^2}{4\eta\zeta^2\pi^2 + 4\eta^2\zeta\pi t_{acq}}}. \tag{3.11}$$

   The ENC related to the detector leakage current has been calculated for three acquisition times $t_{acq}$: 1 µs, 0.5 µs and 0.3 µs, as presented in Fig. 3.4. The

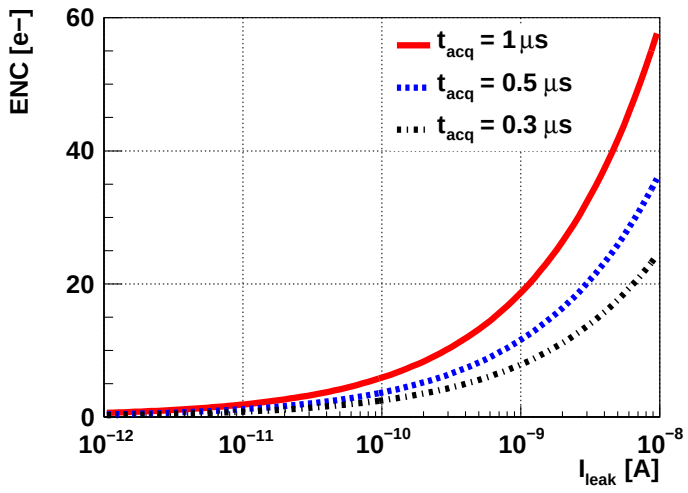



**Figure 3.4:** Calculated noise originating from detector leakage current.

preamplifier was optimized assuming maximum sensor leakage current of 10 pA, what gives the calculated ENC related to sensor leakage current below 4 $e^-$.

The noise terms related to the transistors M1 (Eqs. 3.1, 3.7–3.9) and M3 (Eq. 3.10) as well as shot noise of the detector leakage current (Eq. 3.11) are shown in Fig. 3.5. One can notice the dominant noise terms originate primarily from the input transistor M1 and also from the transistor M3. The parallel noise related to the detector leakage current is relatively low, assuming the acquisition time $t_{acq}$ of 1 µs and the detector leakage current of 10 pA.

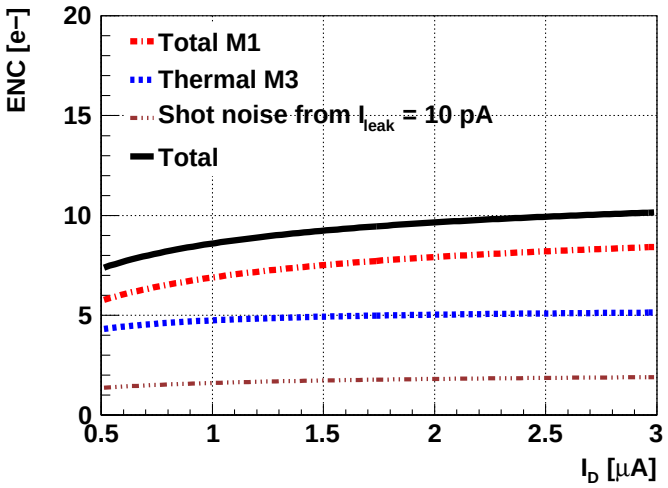



**Figure 3.5:** Calculated ENC originating from the preamplifier operating in the acquisition phase. Following numerical values have been used: acquisition time $t_{acq}$ of 1 µs and the detector leakage current of 10 pA has been assumed.

Finally, the nominal bias current $I_D$ of 2 µA has been chosen. This choice has been driven by compromising the two following factors:

1. Power consumption, which increases for higher $I_D$. For a nominal bias current of 2 µA and power supply voltage of 2.5 V the power consumption is estimated about 10 µW per pixel.

2. Reduction of the signal integration time constant:

$$\tau_i = \frac{C_{int}C_{out} + C_f(C_{int} + C_{out})}{C_{int}g_{ds3acq} + C_f(g_{ds3acq} + g_{m1})}. \tag{3.12}$$

The time interval needed for the signal integration defines a minimum acquisition time $t_{acq}$ and consequently, the sensitivity of the total ENC to the parallel noise

sources (the longer acquisition time, the greater influence of the detector leakage current noise). For nominal bias current of 2 μA and other parameters as listed in Tab. C.1 the integration time constant of 80 ns has been estimated .

For the nominal parameters of the circuit described above, the expected ENC is below 10 $e^-$. The results presented in Fig. 3.5 show that the noise performance of the preamplifier is dominated by the channel thermal noise of input MOS transistor. In addition, the influence of the cascode load transistor M3 is significant and can not be omitted. This noise should be added to the noise term originating from preamplifier operating in the reset phase in order to estimate total noise of the preamplifier operating in the acquisition phase.

### 3.4.2 Noise related to the preamplifier operating in the reset phase

The noise in the reset phase is due to the channel thermal noise of transistors M1, M3, M4 and M6. During the reset phase the feedback capacitor $C_f$ is discharged by a feedback transistor M4 biased with the reset current $I_{\text{reset}}$. Therefore, the preamplifier transfer functions for the parallel and series noise sources differs from the one in the acquisition phase. One should remember that the reset phase transfer functions strongly depends on the reset current $I_{\text{reset}}$, which sets the feedback transistor transconductance $g_{m4}$ and, consequently, the active feedback resistance equal to $1/g_{m4}$. Taking into account the equations describing the spectral densities of channel thermal noise related to MOS transistors listed above, and applying the preamplifier transfer function C.9 and C.15, one can calculate the output RMS noise values. It is assumed that while switching the preamplifier from reset to the acquisition phase the output noise is fed back to the input node and then subsequently transferred to the preamplifier output with the acquisition phase transfer function. This effect is approximated by additional term in the preamplifier transfer functions for the reset phase, as defined by Eq. C.21. This approximation brings about the expressions for the RMS noise values — Eqs. C.22–C.25 — describing how the reset phase influences the amplifier during the acquisition phase. This noise is expressed in ENC in order to compare it with the noise components originating from the acquisition phase. Fig. 3.6 shows the reset phase noise as it is seen in the acquisition phase for wide range of $I_{\text{reset}}$. Based on these results, the minimal noise of 26 $e^-$ can be obtained for reset current of 10 nA. According to noise analysis presented above, in the real circuit the reset current has been left programmable from 10 nA to 300 nA keeping the noise level below 70 $e^-$ .

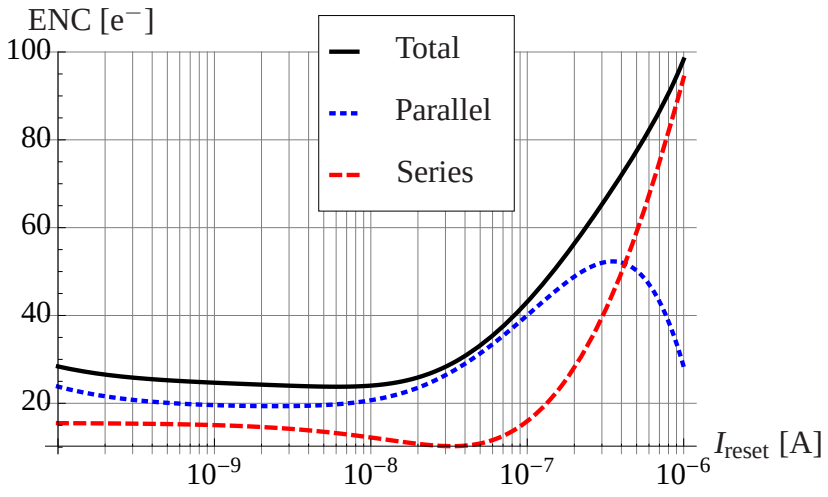



**Figure 3.6:** Calculated reset phase noise seen in the acquisition phase.

### 3.4.3 Total noise of the preamplifier

As one can notice, total noise that originates from the reset phase, manifests itself in the acquisition phase at a level much higher that the noise of 10 $e^-$, as shown in Fig. 3.7. ENC estimated to be generated in the acquisition phase. Furthermore, it increases for higher values of reset current, what suggests the $I_{reset}$ should be set to low values.

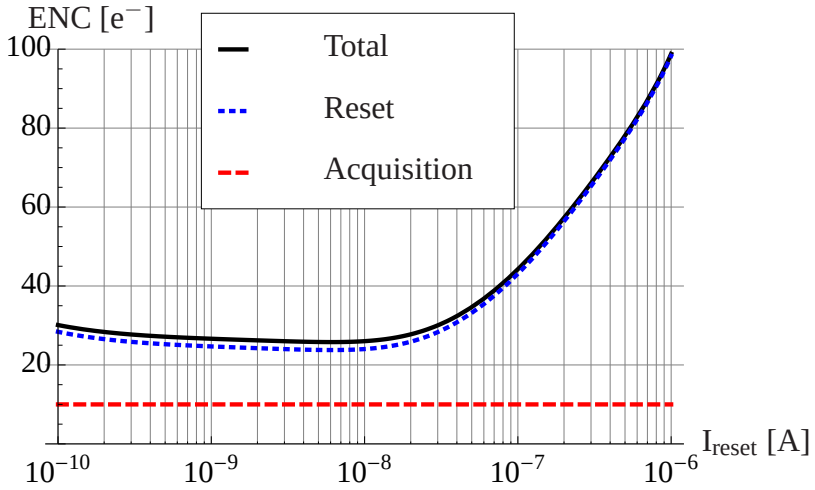



**Figure 3.7:** Calculated ENC originating from the reset phase as it it seen in the acquisition phase compared with calculated acquisition phase noise.

Taking into account the estimated noise of 26 $e^-$ originating form the reset phase and estimated noise of 10 $e^-$ coming from the acquisition phase, the total ENC of 28 $e^-$ has been found. In the Appendix C it is shown how would the reset output noise behave

for a given $I_{reset}$ if measured in the reset phase. This estimation is compared with the measurement results further in this chapter. In such a case an opposite noise dependence on $I_{reset}$ is observed, namely the output noise decreases for higher reset current. This happens due to the fact that the gain of the preamplifier working in the reset phase approaches zero as $I_{reset}$ increases, hence the noise is attenuated.

## 3.5 Experimental results

A demonstartor chip, called Amorphous Frame Readout Pixel (AFRP), has been designed and manufactured in 0.25 µm CMOS process. It contains a matrix of 64 by 64 pixels, where each pixel includes a preamplifier stage working as a gated integrator. This configuration was chosen to study the possible benefits in noise performance that come due to the low duty cycle of the accelerator. In the demonstrator chip, no additional pulse shaping nor digitization was implemented, thus it was not meant to investigate the time stamping issues mentioned earlier.

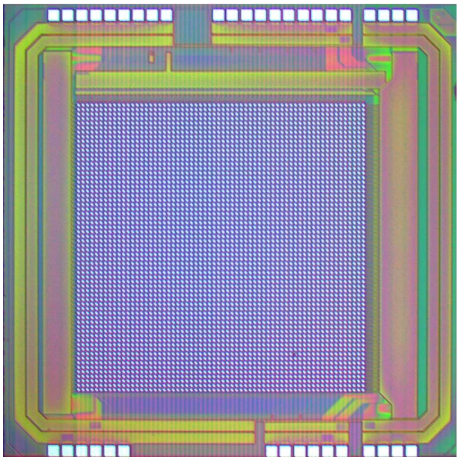


**Figure 3.8:** Amorphous Frame Readout Pixel chip.

A photo of the AFRP demonstrator chip is shown in Fig. 3.8. A matrix of 4096 pixels with pixel area of 40 µm by 40 µm, are read out serially through a multiplexer. Due to the limited number of three metal layers in the process used for manufacturing of the demonstartor chip, the active area of the input electrode is only 20 µm by 20 µm, which is one forth of the pixel area. Using more metal layers one can easily imagine designing the sensor area equaling the pixel size. The analog and digital grounds and power supply buses are separated to reduce the noise in the preamplifier. Two clock signals to read out rows and columns of the chip, as well as 10MHz master readout clock are supplied

externally using the Low Voltage Differential Signaling (LVDS) standard. The readout time of the full pixel matrix is less than 2.5 ms (600 ns/pixel, in this time period output voltage is sampled 6 times). The 10 µm thick a-Si sensor was deposited directly on the AFRP chip surface. The deposition was done at the Institute of Microengineering[1] by using Plasma Enhanced Chemical Vapor Deposition process [80].

### 3.5.1 Noise performance of the bare chip

A bare AFRP chip was tested to characterize the noise performance of its 4096 pixels. The noise on each pixel was measured as the RMS value of the output voltages, taken from 200 chip scans, after subtracting the voltage pedestals (mean value of 200 measurements) and expressed in ENC. The average noise over all pixels on the AFRP chip as a function of reset current is shown in Fig. 3.9. An estimated ENC trend agrees with the measurement

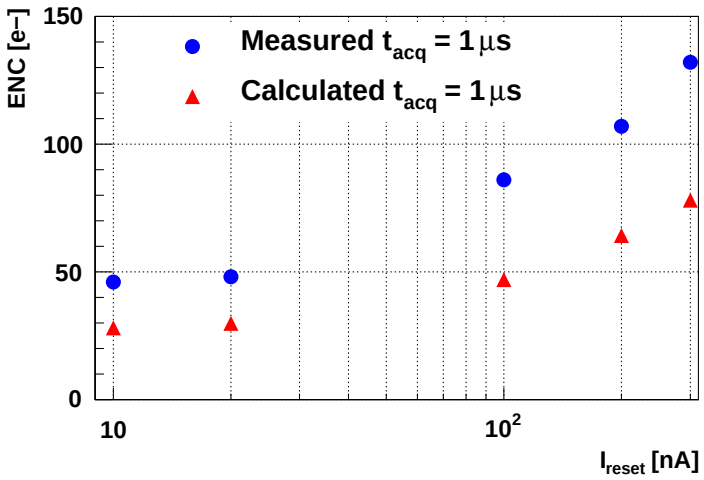



**Figure 3.9:** Calculated and measured noise of the bare AFRP chip. The measured noise is an average value over 4096 pixels taken from 200 chips scans.

results, however the latter one is higher than it was modeled. The difference between the calculated and measured noise increases proportionally with increasing the reset current $I_{reset}$. The noise measured in the reset phase as well as the calculated one are shown in Fig. 3.10.

[1]Ecole Polytechnique Fédérale de Lausanne , Institute of Microengineering, Photovoltaics and thin film electronics laboratory (EPFL-STI-IMT-NE, PV-LAB), Rue Breguet 2, CH-2000 Neuchâtel, Switzerland

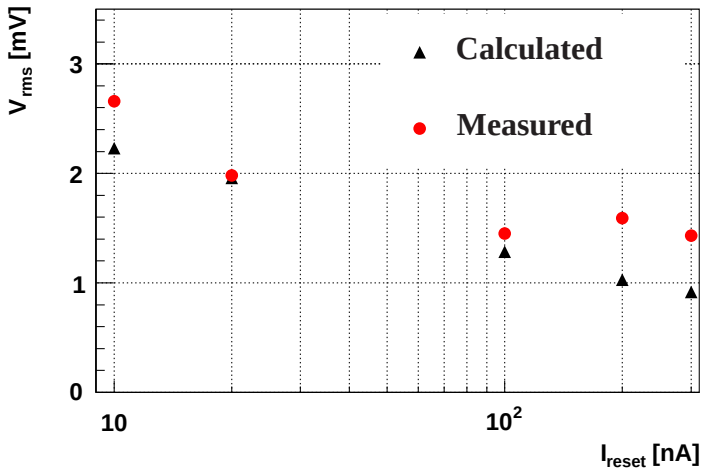



**Figure 3.10:** Calculated and measured noise of the preamplifier operating in the reset phase. The measured noise is an average value over 4096 pixels taken from 200 chips scans.

The model agrees reasonably well with the test results, what proves correct description of the reset phase noise. Comparing the measured and the calculated noise, one should keep in mind that in the presented chip the noise is very low anyway. Therefore, one cannot exclude, that the measured noise is also affected by other noise sources, like coupling through the silicon substrate, noise injected through the power supply lines and electromagnetic interferences. Another aspect to be kept in mind when comparing the calculated and the measured noise level is related to the estimation of the transfer function in the reset phase and in the acquisition phase. For estimation of the measured ENC the nominal gain about $1/C_f$ was assumed, using the nominal value of the feedback capacitance, equal to 1.3 fF. Any small parasitic capacitance on the level of a fraction of fF may introduce a significant error to the estimated gain of the circuit.

Fig. 3.11 shows the map of noise measured for acquisition time $t_{acq}$ of 1 µs and the reset current of 10 nA. It is worth noting that the noise performance is uniform over whole chip area. Fig. 3.12 shows the distribution of noise for 4096 pixels. The mean noise of 49 e- and the standard deviation of 4 e- have been evaluated based on measurement results.

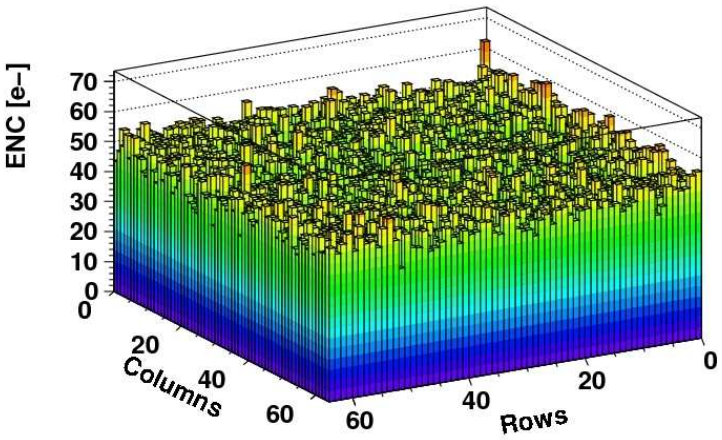



**Figure 3.11:** Bare chip noise map for $I_{reset}$ = 10 nA and $t_{acq}$ = 1 μs measured during 200 chip scans.

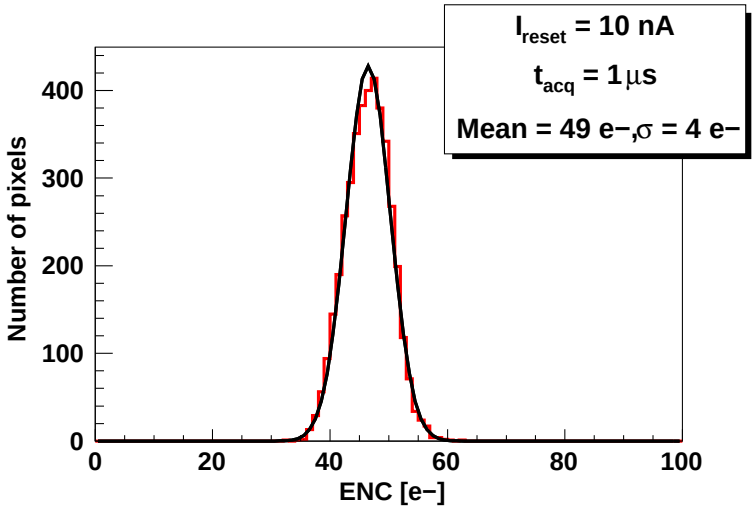



**Figure 3.12:** Bare chip noise spread over 4096 pixels for $I_{reset}$ = 10 nA and $t_{acq}$ = 1 μs.

### 3.5.2 Noise performance of the TFA structure

The noise performance of the TFA structure has been investigated in the same way as for the bare AFRP chip, namely RMS value of the output voltage has been evaluated from 200 chip scans after subtracting voltage pedestals. The a-Si:H diode biased with 55 V introduces additional capacitance at the preamplifier input, which was included in the model. First important remark is that the measured leakage current turned out to reach a level of 1 nA, which was about two orders of magnitude more, than the expected

value of 10 pA. Thus, the shot noise originating from the sensor leakage current was recalculated, as shown in Fig. 3.13 and Fig. 3.14.

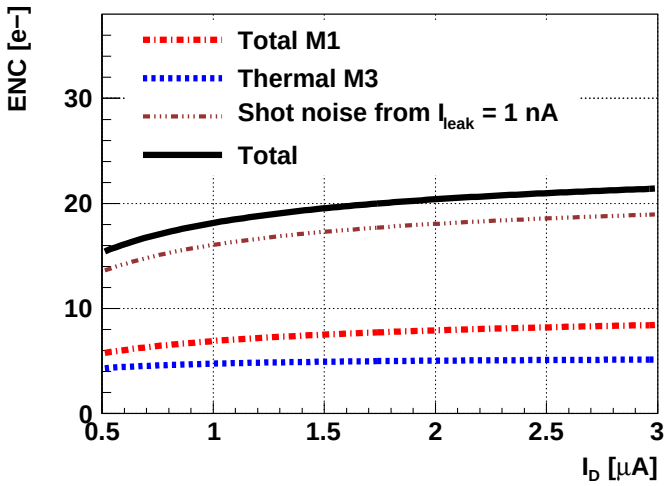



**Figure 3.13:** Recalculated ENC originating from the preamplifier operating in the acquisition phase. Following numerical values have been used: acquisition time $t_{acq}$ equals to 1 μA and the detector leakage current of 1 nA (as measured).

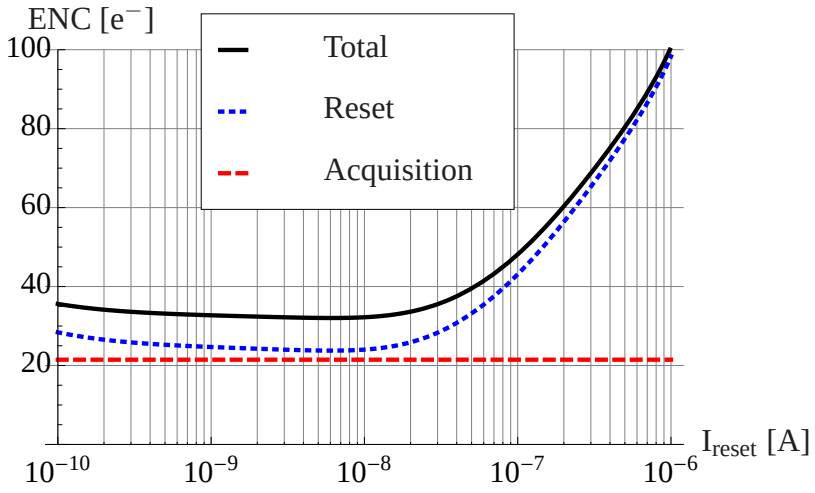
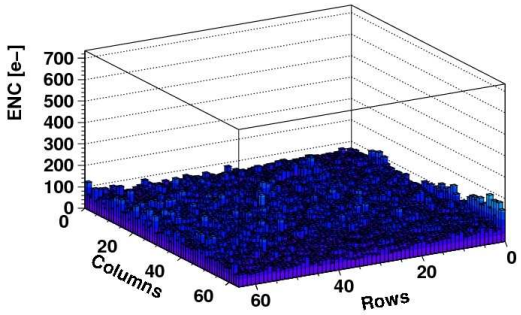


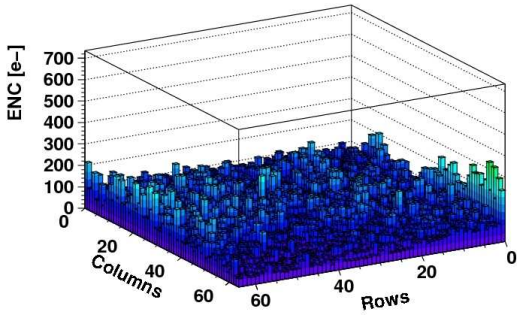

**Figure 3.14:** Recalculated ENC originating from both phases: reset and acquisition, including measured detector leakage current of 1 nA.

The noise maps as measured on the TFA structure for various values of acquisition time $t_{acq}$ are presented in Figs. 3.15a–3.15c. These noise maps show much larger spread

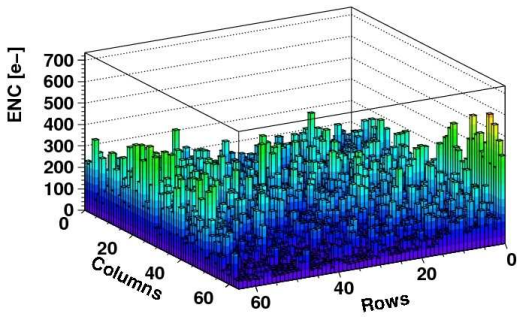
across the pixel array compared to the bare AFRP. This effect is even more pronounced for the longer acquisition times, which indicates that the spread is mainly due to the variation of the sensor leakage current.




**(a)** $t_{acq}$ = 0.3 µs



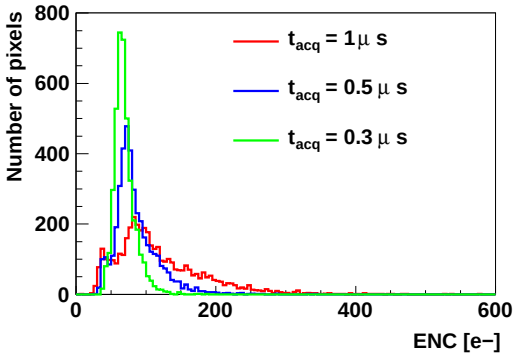

**(b)** $t_{acq}$ = 0.5 µs



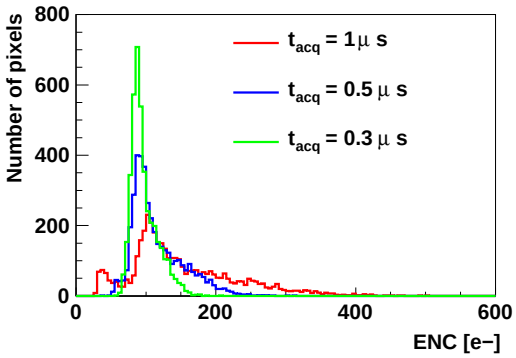

**(c)** $t_{acq}$ = 1 µs

**Figure 3.15:** Map of the noise measured on the TFA structure for a reset current of 10 nA and an a-Si diode bias of 55 V.

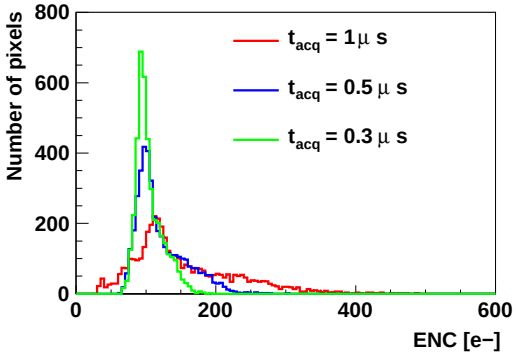
Figs. 3.16a–3.16c show distributions of measured noise for various acquisition times. One can notice that besides relatively narrow peaks, one observes long tails corresponding to pixels with noise much higher than the average. These effects are most likely related to the leakage current variations, due to non-uniformity of the sensor–ASIC interface.




**(a)** Reset current of 10 nA




**(b)** Reset current of 100 nA




**(c)** Reset current of 200 nA

**Figure 3.16:** Noise spread on 4096 pixels of the TFA structure for diode bias voltage of 55 V.

Fig. 3.17 shows comparison of calculated and measured noise of the TFA structure, taking into account the most probable values of measured ENC distributions. The calculated values are taken for the sensor leakage current of 1 nA.

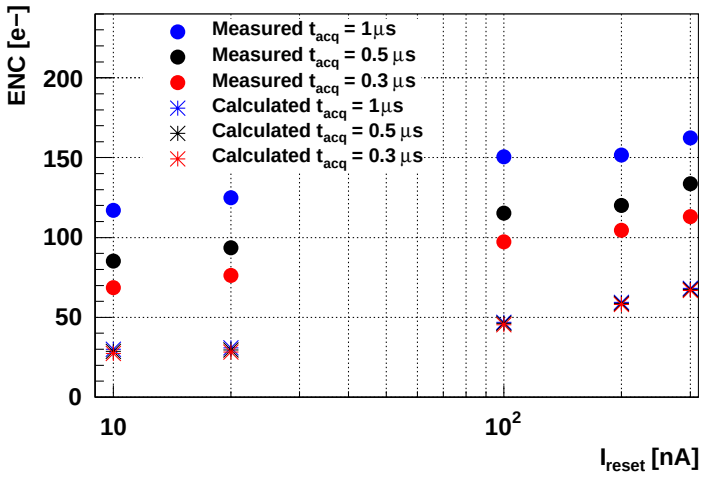


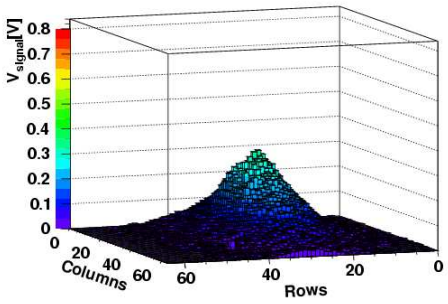

**Figure 3.17:** Calculated and measured most probable noise of the TFA structure as a function of reset current. The 10 μm thick a-Si diode was biased with 55 V.

### 3.5.3 Gain calibration using a 405 nm blue laser

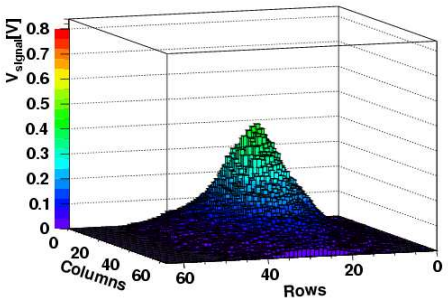
As mentioned earlier estimation of the measured ENC depends strongly on the assumed gain. Experimental calibration of the gain of the described circuit is not at all a trivial task. One cannot use electronic pulses, because for such small feedback capacitance one cannot estimate parasitic charge injection through stray capacitances. Using charge generated by X-rays in a-Si diode does not work, because of unknown trapping of charge in amorphous silicon. Therefore, an indirect method using laser light was applied.

The TFA device was tested with the 405 nm blue laser pulses. The signals obtained on 10 μm a-Si diode, reversely biased with voltages from 15V to 60V, have been measured. In order to minimize the influence of the sensor leakage current on the front-end noise performance, the acquisition time was set to a short value of 300 ns. During this time periods the blue laser was triggered to fire a pulse on the TFA surface and the signals were read out from all 4096 pixels. Twenty chip scans were made with laser pulses detected on the TFA. In order to illustrate the sensor response $V_{signal}$ to the laser pulse, the pedestals,

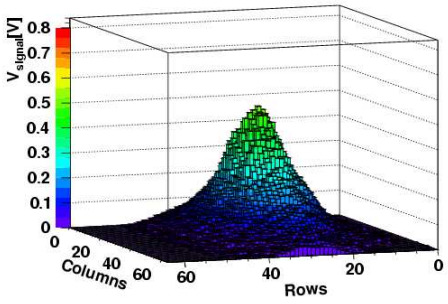
measured with no incoming laser pulses, were subtracted. Fig. 3.18 shows the sensor responses averaged over 20 scans for different bias voltages, from 15 V to 60 V.



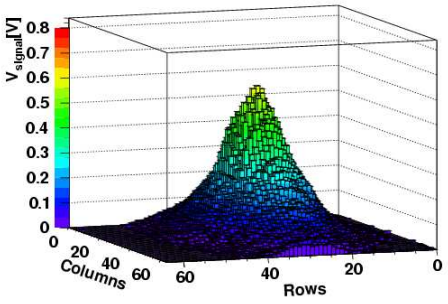

**(a)** a-Si diode bias voltage 15 V



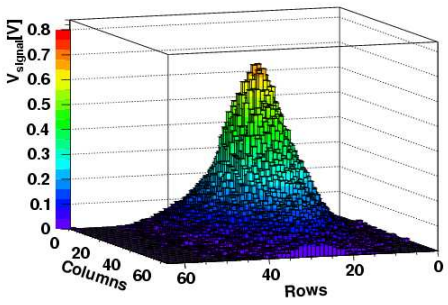

**(b)** a-Si diode bias voltage 25 V



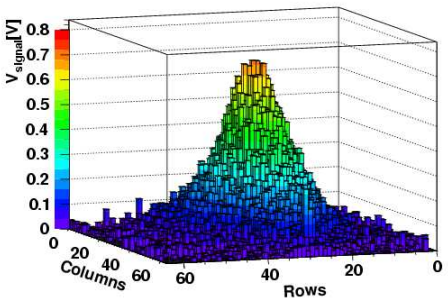

**(c)** a-Si diode bias voltage 35 V




**(d)** a-Si diode bias voltage 45 V




**(e)** a-Si diode bias voltage 55 V




**(f)** a-Si diode bias voltage 60 V

**Figure 3.18:** Signals from 405 nm blue laser, obtained on 10 μm thick a-Si diode biased with a voltage of 15–60 V.

The full depletion bias voltage of the 10 μm thick sensor was measured by recording the maximum response $V_{\text{max signal}}$ to the laser pulse as a function of diode reverse bias voltages $V_{\text{a-Si bias}}$. This method, demonstrated in [78], is based an assumption that the collected charge is proportional to the thickness of the depleted layer. As shown in

Fig. 3.19, the sensor response to a blue laser pulse increases as a square root of the applied voltage, and starts to saturate for a bias voltage of 55 V. This result agrees with Ref. [78], where the full depletion bias voltage for a-Si sensor with a thickness d is estimated as $0.48 \times d^2$, leading to about 48 V for a 10 μm thick diode.

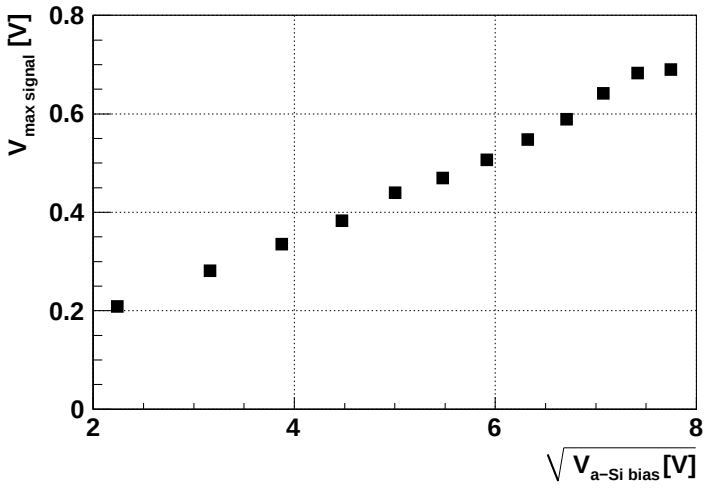



**Figure 3.19:** Maximum response of the TFA structure to the 405 nm blue laser pulse for $I_{reset}$ = 10 nA and $t_{acq}$ = 0.3 μs.

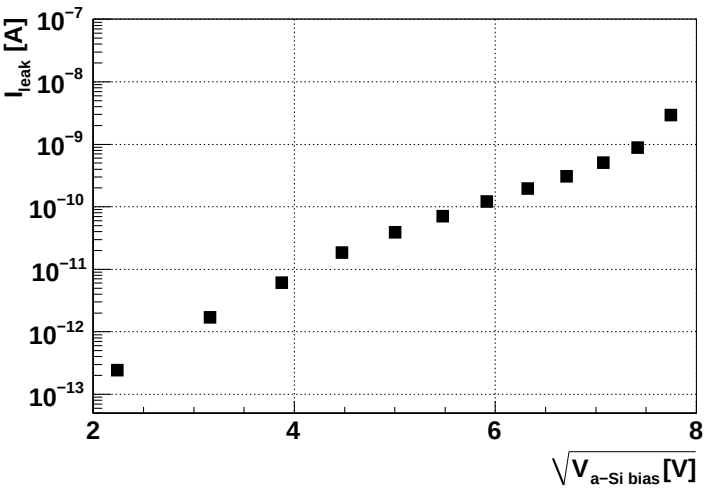



**Figure 3.20:** Average leakage current per pixel measured on 10 μm thick a-Si sensor.

The response of the TFA structure to a 405 nm blue laser was cross-calibrated with the response obtained on TFA sensors developed on the MacroPad chip [47], for which

the calibration factors are known from measurements of X-rays. As a result, a gain of 713 mV/fC was found compared to the simulated gain of 800 mV/fC.

The average leakage current per pixel was measured as a function of the a-Si:H reverse bias voltage. As shown in Fig. 3.20, for the fully depleted a-Si sensor, biased with 55 V ($\sqrt{V_{a-Sibias}} = 7.4$ V), the leakage current per pixel is about 1 nA, which is two orders of magnitude higher compared to the level of 10 pA, assumed for the preamplifier design.

## 3.6 Conclusions on the AFRP ASIC development

A 64×64 pixels array based on TFA technology has been designed, manufactured and tested. The readout electronics has a gain of 713 mV/fC and a power consumption of 10 μW per pixel. The ENC less than 70 $e^-$ has been measured on TFA structure expected to provide signal of about 370 $e^-$ generated by MIP in 10 μm thick a-Si sensor. One can notice the noise performance of bare AFRP ASIC is higher than expected, but it is satisfactory taking into account the expected response signal from the a-Si sensors. The noise performance of the present TFA prototype is limited by the leakage current. Since the preamplifier was designed and optimized for sensor leakage current of 10 pA, the readout electronics cannot handle a 1 nA leakage current for acquisition times longer than 1 μs. The TFA structure was tested with 405 nm blue laser pulses, which were triggered precisely during the acquisition phase of the preamplifier. Images of the laser spot provide a solid proof of principle that the developed pixel detector structure works. The main problem of the present prototype is related to the excessive leakage current, which strongly depends on the quality of an a-Si–ASIC interface. Therefore, further improvements of the process of sensor material deposition on the ASIC, including the planarization of the ASIC surface, are needed.

# Summary

In the thesis the designs and test results of two prototype front-end circuits for tracking and vertex detectors for future high energy particle physics experiments have been presented. The requirement specifications are driven by experimental environments as expected in the future accelerators; SLHC and CLIC. The common requirements for both designs are low noise, high precision, low power and radiation hardness. The circuits have been designed and manufactured in a 0.25um CMOS process from IBM, employing special design techniques to ensure required radiation hardness.

One of the key aspect of the ATLAS detector upgrade is development of a front-end ASIC for reading out the silicon strip detectors. At this stage, a front-end chip with full functionality serving as a test vehicle for the SSD development is also needed. For this reason a prototype front-end chip, called ABCN-25, has been designed and manufactured in IBM 0.25 μm CMOS process. This prototype employs the binary readout architecture, which provides all functions required for processing the signals from 128 strips of a SSD in the ATLAS Inner Detector upgrade. The design of the analog front-end circuitry has been presented in Chapter 2. The emphasis has been put on the circuits designed by the author, namely the digital-to-analog converters and the calibration circuit. The impact of stochastic and systematic mismatch on the circuit performance has been taken into account. The safety factor due to radiation damage effects has been also accounted. The test results of manufactured ASICs have shown correct functionality of the ABCN-25 chip. The analog blocks have been measured after irradiation of the chip up to 100 Mrad. The functionality of the ABCN-25 ASIC after irradiation has been proven. However, post-irradiated degradation in accuracy of matched devices has been observed, even if the enclose gate geometry layout of NMOS devices was implemented. The obtained results lead us to a conclusion that increasing of DAC resolution will be necessary to ensure sufficient precision after irradiation. These conclusions will be taken into account in the design of next generation ASIC to be implemented in the more advanced process, such as IBM 0.13 μm CMOS.

The Thin Film on ASIC technology is a possible option for the vertex detector at CLIC. Author's work on circuit design and noise optimization of the front-end electronics has been described in details in Chapter 3. The demonstrator chip, called AFRP, containing an array of $64 \times 64$ pixelized front-end circuits has been fabricated in the IBM $0.25\,\mu m$ process. A test system has been developed by the author to characterize the noise performance of the bare chip and the complete TFA device, composed of $10\,\mu m$ thick amorphous silicon sensor deposited on top of the readout ASIC. The test results have been reported and concluded. The functionality and low noise performance of the AFRP chip have been demonstrated. A precise image of the laser spot has provided a solid proof of principle for the developed pixel detector concept. However, the noise performance of the TFA prototype has been found to be limited by excessive sensor leakage current. This issue has been associated with the quality of the a-Si–ASIC interface. It has been concluded that in order to employ the TFA technology in future particle physics experiments further improvements of the technology of sensor deposition on ASIC, including the planarization of the ASIC surface, are needed.

# Appendix A

# EKV model of MOSFETs

The EKV MOS transistor model has its roots in the development of electronic watches at CEH [1] in the late sixties in Switzerland. In order to sustain the watches' quartz oscillator, the transistors in the analog circuitry were biased with a very low current. This allowed then to obtain a lifetime of a few years from a single button-sized cell battery. However, the measurements were showing a very strange behavior of the MOS transistor biased with a low current in a range of 1 μA, not predicted by of that time theory. Thus, the new models were aiming at precise description of a voltage-current relationship for the MOS transistor in the weak inversion — biased with low currents. However, even in micropower analog circuits, not all the transistors should be biased in a weak inversion, hence the need for a model, continuous from weak to moderate up to strong inversion region was undisputed. In the 1980's, an adequate MOS transistor model was developed by C. C. Enz, F. Krummenacher and E. A. Vittoz and named from the initials of the authors as "EKV model".

The EKV model is a fully analytical MOS transistor model, that provides all the large- and small-signal variables of the MOS transistor, such as transconductance and intrinsic capacitances, offering continuity in all regions of operation, namely weak, moderate and strong inversion, conduction and saturation. The fundamental concepts of the EKV model together with a mathematical description can be found in Ref. [83]. In this thesis, the MOS transistor modeling, based on the EKV model, is employed in the noise analysis of the analog preamplifiers. One should keep in mind the main noise source of the preamplifier is related to the input MOS transistor working in saturation and between weak and moderate inversion. Under these conditions, the EKV model can be simplified with respect to two

[1] French acronym for Watchmakers Electronics Center

**Table A.1:** Parameters used for modeling of the MOS transistor designed in IBM 0.25 μm technology.

| MOS transistor model parameters | | | |
|---|---|---|---|
| Symbol | Description | Value | Units |
| $n$ | Slope factor | 1.45 | - |
| $t_{OX}$ | Effective gate oxide thickness | $6 \times 10^{-9}$ | m |
| $C_{OXU}$ | Gate-to-Source capacitance per unit area | 5.56 | $\mathrm{fF}/\mu\mathrm{m}^2$ |
| $C_{OVU}$ | Gate-to-Diffusion capacitance per unit gate width | 0.4 | $\mathrm{fF}/\mu\mathrm{m}$ |
| $K_P$ | Transconductance parameter | 300 (NMOS)<br>75 (PMOS) | $\mu\mathrm{A}/\mathrm{V}^2$<br>$\mu\mathrm{A}/\mathrm{V}^2$ |
| $W$ | Transistor gate width | defined by designer | $\mu$m |
| $L$ | Transistor gate length | defined by designer | $\mu$m |
| Noise parameters | | | |
| $\Gamma$ | Excess noise factor | 1.3 (NMOS, L$\geq$500 nm)<br>1.25 (PMOS, L$\geq$400 nm) | -<br>- |
| $K_a$ | Flicker noise coefficient | $6 \times 10^{-27}$ (NMOS)<br>$1 \times 10^{-27}$ (PMOS) | $\mathrm{C}^2/\mathrm{m}^2$<br>$\mathrm{C}^2/\mathrm{m}^2$ |
| Physical constants | | | |
| $k$ | Boltzmann's constant | $1.3806 \times 10^{-23}$ | J/K |
| $q$ | Magnitude of electronic charge | $1.6021 \times 10^{-19}$ | C |
| $T$ | temperature | 300 | K |

parameters: the slope factor $n$ and the electron surface mobility $\mu_0$. Here, it is assumed that both of the parameters are constant, which is valid as long as the transistor does not enter the strong inversion region, where $n$ and $\mu_0$ becomes bias dependent. The MOS transistor model parameters specified for the IBM 0.25 μm technology as well as the physical constants used in calculations are defined in table A.1.

An estimation of MOS transistor transconductance $g_m$ and gate capacitance $c_g$, for a given drain current $I_D$ and transistor gate size $W \times L$, is essential to ensure the proper noise analysis of the front-end preamplifier. These parameters are modeled as presented below.

1. Modeling of the transistor transconductance $g_m$:

   The general expression for the MOS transistor drain current in saturation can be calculated as described by Eq. A.1 (see pp. 17 and 27 of Ref. [84]):

$$I_D = \begin{cases} \frac{K_P}{2}\frac{W}{L}(V_{GS} - V_{th})^2 & \text{in strong inversion (S.I.)} \\ I_{D0} e^{\frac{V_{GS}}{\varsigma U_t}} & \text{in weak inversion (W.I.)} \end{cases} \tag{A.1}$$

where $V_{th}$ is a threshold voltage, $V_{GS}$ is a gate-source voltage, $I_{D0}$ is drain current at $V_{GS} = V_{th}$, the $U_T$ equals $kT/q$, $\varsigma$>1 is nonideality factor, $K_P$, $W$, $L$ and $n$ are defined in Tab. A.1.

This expression defines the drain current only in the strong and weak inversion regions, leaving the moderate inversion region with no valid equation. For this reason the EKV model provides a proper interpolation of the drain current between the two known asymptotic regions mentioned above. In order to find the interpolation function, the current was normalized to obtain the relation between current and the voltages independent of the transistor sizes and of the technological parameters. The specific current $I_S$, used for the normalization, is described by Eq. A.2 (see pp. 37 of Ref. [85]):

$$I_S = 2n\beta U_T^2, \tag{A.2}$$

where $\beta$ equals $K_P W/L$. Using the specific current $I_S$, the interpolation of transconductance between strong and weak inversion for a given drain current $I_D$ is defined by Eq. A.3

$$G(I_f) = \frac{1}{\sqrt{I_f + \frac{1}{2}\sqrt{I_f} + 1}}, \tag{A.3}$$

where $I_f$ is a forward normalized current, equal to $I_D/I_S$. Finally, the transconductance of the MOS transistor working in saturation is defined for a given drain current $I_D$ as follows (Eq. A.4):

$$g_m = G(I_f)\frac{I_D}{nU_T}. \tag{A.4}$$

2. Modeling of the intrinsic gate capacitance $c_g$:

The intrinsic gate capacitance $c_g$ of the MOS transistor working in saturation consists of the three following components (A.5, A.7):

(a) Gate-to-Source capacitance $C_{GS}$, defined as:

$$C_{GS} = C_{GSU} WL, \tag{A.5}$$

where $C_{GSU}$ is a unitary Gate-to-Source capacitance, described by Eq. A.6

$$C_{GSU} = C_{OXU}\left(\frac{1}{I_f G(I_f)} + \frac{3}{2}\right)^{-1}, \tag{A.6}$$

and $C_{OXU}$ is an unitary gate capacitance equal to $\varepsilon_{OX}/t_{OX}$, $\varepsilon_{OX}$ is the dielectric constant of $SiO_2$ and $t_{OX}$ is defined in table A.1,

(b) Gate-to-Bulk capacitance $C_{GB}$, represented by:

$$C_{GB} = C_{GBU} WL, \tag{A.7}$$

where $C_{GBU}$ is a unitary Gate-to-Bulk capacitance, defined by Eq. A.8

$$C_{GBU} = C_{OXU}\frac{n-1}{n}\left(1 - \frac{if G(I_f)}{1+\frac{3}{2}I_f G(if)}\right). \tag{A.8}$$

(c) Gate-to-Drain and Gate-to-Source overlap capacitances are calculated as

$$C_{OV} = 2C_{OVU} W, \tag{A.9}$$

where $C_{OVU}$ is a Gate-to-Diffusion capacitance per gate width, defined in Tab. A.1.

Finally, the total intrinsic gate capacitance is calculated as sum of the three:

$$c_g = C_{GS} + C_{GB} + C_{OV} \tag{A.10}$$

# Appendix B

# Noise in MOSFETs

Noise is a random process, which means that its instantaneous amplitude cannot be predicted, even if the past values are known. A noise signal x(t) is a quantity that has a zero mean value $\overline{x(t)}$ and a nonzero mean square value $\overline{x(t)^2}$. As an example, consider the drain current in the MOS transistor biased with fixed noiseless terminal voltages. The total drain current $i_{DS}(t)$ consists of an ideal bias current $I_{DS}$ and the noise component $i_n(t)$, which is expressed by Eq. B.1:

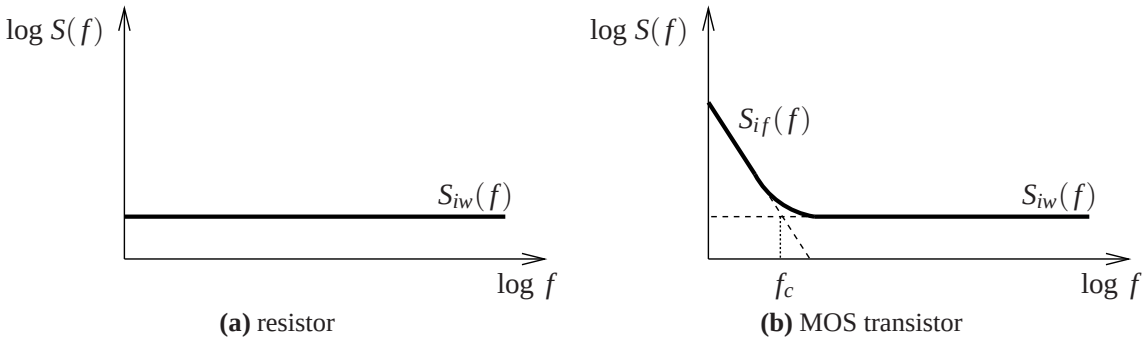
$$i_{DS}(t) = I_{DS} + i_n(t). \tag{B.1}$$

The $i_n$ current has zero average value and one cannot foresee its instantaneous value at a given $t$. However, noise can be modeled statistically and characterized by predicting the mean square value, denoted by $\overline{x_n^2}$, and the root mean square value, $\sqrt{\overline{x_n^2}}$.

In the electronic circuits, very often the fluctuating signal comes across amplifier and filter stages. In this case a relationship between the noise RMS values measured at the output and at the input of electronic device depends on transfer function of an amplifier and a filter stages. Therefore, the noise analysis is based on the analytical description of current and voltage equivalent noise sources as well as the transfer functions of the amplifying and filtering stages, which influences the noise figure as the fluctuating quantity passes by.

## B.1 Noise spectrum

By employing a Fourier analysis of a random noise signal $x(t)$, where $x(t)$ represents current $i_n(t)$ and voltage $v_n(t)$ noise signals, the power spectral density $S_x(f)$ of $x(t)$ can be defined ([82], pp. 30–33), so that $S_x(f)\Delta f$ represents the mean square value of noise




**(a)** resistor **(b)** MOS transistor

**Figure B.1:** Noise spectrum examples.

waveform $x(t)$ in the frequency interval $\Delta f$ around center frequency $f$ ([86], pp. 411). Power spectral density $S_x(f)$ obeys the following theorems ([82], pp. 34–35):

1. The mean square value of the noise signal $x(t)$, which has a Power Spectral Density (PSD) $S_x(f)$, can be calculated as

$$\overline{x^2} = \int_0^\infty S_x(f)\,df \tag{B.2}$$

2. For $\overline{x^2}$ to exist, the integral B.2 must converge.

3. If the noise signal $x(t)$ with a PSD $S_x(f)$ is applied to the input of an amplifier of complex voltage gain $g(f)$, then the output noise signal $y(t)$ has a mean square value

$$\overline{y^2} = \int_0^\infty S_x(f)\,|g(f)|^2\,df. \tag{B.3}$$

The PSD for current ($S_i(f)$) and voltage ($S_v(f)$) noise is expressed in $A^2/Hz$ and $V^2/Hz$, respectively. The entire PSD of noise for certain devices can be constant over a frequency range, as it is for resistors (see $S_{iw}(f)$ in Fig. B.1a), or can vary over a frequency range as it is for transistors (see a combination of terms $S_{iw}(f)$ and $S_{if}(f)$ depicted in Fig. B.1b). In a resistor there is only one source of noise, namely the thermal noise originated from thermal motion of carriers in the resistor. The MOS transistor shows a more complex noise spectrum caused by a superposition of several physical processes. Each of these processes can be represented by an equivalent noise source — current or voltage — characterized by a given PSD.

# B.2 Noise spectrum of the MOS transistor

## B.2.1 Thermal noise

In 1927, the first experiments that showed the random variation of potential between the ends of the conductor were made by John Bertrand Johnson, who also provided the formula describing the behavior of observed noise [87]. One year later, Harry Nyquist derived the theoretical basis of Johnson's formula, based on the principles of quantum and statistical mechanics [88]. Thus, thermal noise is also called "Johnson noise" or "Johnson–Nyquist noise". It appears on the terminals of any conductor in equilibrium, regardless of applied voltage, due to the random motion of carriers [82]. The noisy conductor of pure resistance R and of absolute temperature T can be represented as an Thevenin equivalent circuit [89] consisting of ideal (noiseless) resistor $R$ in series with an equivalent noise voltage source $v_t$, as depicted in Fig. B.2. The corresponding power

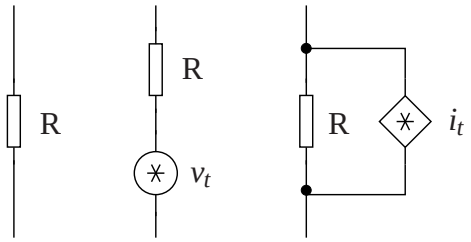



**Figure B.2:** Thermal noise of the resistor

spectral density is described by Eq. B.4:

$$S_{vth-R}(f) = 4kTR, \tag{B.4}$$

where k is Boltzman's constant defined in Tab. A.1. This representation can be converted to the Northon equivalent circuit [90], consisting of noiseless resistance connected in parallel with current noise source $i_t$, which has a PSD described by Eq. B.5:

$$S_{ith-R}(f) = \frac{4kT}{R}. \tag{B.5}$$

As proven in [82], equations B.4 and B.5 are valid up to infrared frequencies of $6 \times 10^{12}$ Hz at the room temperature of 300 K. In this range the PSD does not depend on frequency, exhibiting a flat line in Fig. B.1a, and is said to be *white* noise.

In case of the MOS transistor, the same noise phenomenon occurs in the conducting channel between drain and source, which is formed in the substrate under the transistor

gate biased with appropriate gate voltage. This resistive channel enables a current flow between drain and source terminal. By analogy with the resistor, the random motion of free carriers within the channel generates noise at the device terminals. The thermal noise of MOS transistor is widely characterized in Refs. [82], [86], [91], [85]. As shown in [83], for long channel MOS devices operating in saturation region, the noise due to thermal motion of charge carriers in the transistor channel can be modeled by a equivalent current noise source connected between the drain and source terminals, as shown in Fig. B.3, with a power spectral density

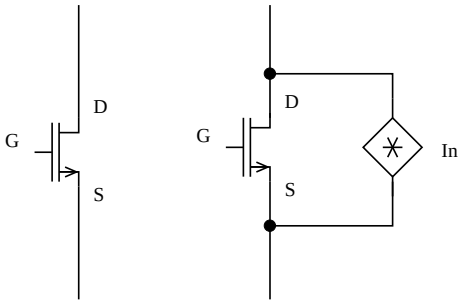



**Figure B.3:** Thermal noise of the MOS transistor

$$S_{ith}(f) = 4kTG_{Nth}, \tag{B.6}$$

where $G_{Nth}$ is the equivalent thermal noise conductance defined as

$$G_{Nth} = \gamma n g_m, \tag{B.7}$$

$\gamma$ is a bias dependent parameter, varying from 1/2 to 2/3 as the long channel transistor is biased from the weak to strong inversion, $n$ is a slope factor (see Tab. A.1) and $g_m$ is transistor transconductance. In order to include into the analysis the thermal excess noise, which is observed for short channel devices, the excess noise factor $\Gamma$ is introduced in modeling the $\gamma$ parameter, as follows

$$\gamma = \Gamma F_n(I_f), \tag{B.8}$$

where $F_n$ is an interpolating function defined as

$$F_n(I_f) = \frac{1}{1+I_f}\left(\frac{1}{2}+\frac{2}{3}I_f\right). \tag{B.9}$$

The $\Gamma$ factor has to be parameterized for a given channel length of a MOS transistor implemented in a particular technology [92]. The $\Gamma$ values for IBM $0.25\,\mu$m technology are shown in Tab. A.1 (see Appendix A).

The additional thermal noise sources are associated with the resistive polysilicon gate and the resistive substrate of the MOS transistor. However, both noise sources can be reduced by proper layout techniques, as described in [93], hence they are not included in the analysis presented in this thesis.

### B.2.2 Flicker noise

The flicker noise has been intensively studied for the past decades. Several theories have been developed in order to explain the origin of this noise, sometimes leading to conflicting conclusions, still leaving several unsolved issues. The exact origin of flicker noise is not known for all devices showing it. It is observed, that its power spectral density is nearly proportional to the inverse of frequency. For this reason flicker noise is also called "1/f" noise. Two dominant theories of an origin the 1/f noise in the semiconducting filaments were introduced by A.L. McWhorter in 1955 and by F. N. Hooge in 1969. The main conclusions related to the MOS transistor are summarized as follows

1. The McWhorter model [94] is based on random fluctuations of the number of carriers in the transistor channel due to trapping and releasing of mobile carriers by traps located near the Si-$SiO_2$ border [86], [85]. McWhorter's theory relates the flicker noise to two types of surface states: "fast" are believed to be located on the semiconductor side of the Si-$SiO_2$ interface, causing rapid recombination of holes and electrons, whereas "slow" are located in the oxide layer itself and exhibit a wide distribution of the trapping time constants [82]. This distribution is related to the trapping process, in which the carriers in a semiconductor sample interact with traps in the surface oxide layer, which involves the tunneling of the carrier from the Si-$SiO_2$ interface to the trap placed in oxide. The fluctuation of the number of trapped carriers causes the fluctuations of the channel free charges, and hence of the channel current. The detailed analysis of the McWhorter model, presented in [85] and [95], provides the following PSD of the equivalent noise voltage in series with the transistor gate

$$S_{vf-M} = \frac{K_M}{C_{OXU}^2 WLf}, \tag{B.10}$$

where $K_M$ is a quantity weakly dependent on bias [85] but dependent on fabrication details in a way that cleaner fabrication processing results in a lower value of $K_M$ [86], $C_{OXU}$ is gate oxide capacitance per unit area, $W$ and $L$ are gate width and length, respectively.

2. The Hooge model [96] attributes the flicker noise to fluctuations of carrier mobility, due to carrier collisions with the crystal lattices. The detailed mechanism of these fluctuations is not known. This theory results in the following PSD of equivalent input noise voltage [85], [86], [95]

$$S_{vf-H} = \frac{K_H}{C_{OXU} W L f}, \tag{B.11}$$

where $K_H$ is bias dependent quantity.

According to [86] it is possible that both effects, namely the carrier number and carrier mobility fluctuations, are presented and correlated in given device, however one or the other effect may be dominant.

Since the majority of the experimental results exhibit the behavior described by McWhorter's model [95], for the design purpose presented in this thesis, the PSD of flicker noise is considered as bias independent, as expressed by B.10.

### B.2.3 Gate induced current noise

At high frequencies, the capacitive coupling between the gate and channel of the MOS transistor has to be taken into account [97]. Random fluctuations of the potential in the transistor channel are coupled to the gate terminal through the oxide capacitance. Thus, the noise current is induced in the gate terminal even if all external voltages are fixed [86]. Following the Ref. [97] and applying the EKV model of the MOS transistor for any operating region, the PSD of the Gate Induced Current (GIC) noise can be defined as:

$$S_{iGIC} = 8\gamma kT g_{gs}, \quad \text{where} \quad g_{gs} = \frac{4(2\pi f)^2 C_{OX}^2}{45 n g_m} \quad \text{and} \quad C_{OX} = C_{OXU} W L, \tag{B.12}$$

### B.2.4 Correlation term

The high frequency GIC noise is correlated the channel thermal noise, thus the correlation term $\overline{S_{ith}S^*_{iGIC}}$ has to be taken into account [97], as follows:

$$\overline{S_{ith}S^*_{iGIC}} = \frac{\gamma}{6} i(2\pi f) C_{OX} 4kT. \tag{B.13}$$

### B.2.5 Generation-recombination noise

Generation-Recombination (G-R) noise occurs whenever free carriers are generated or recombined in a semiconductor material [91]. In a near intrinsic semiconductor material the electron and holes appear and disappear in the following generation and recombination processes:

free electron + free hole $\rightleftharpoons$ electron bound in valence band + energy,

where $\rightharpoonup$ denotes recombination process and $\leftharpoondown$ denotes generation process. The theoretical study of low frequency G-R noise in junction-gate field-effect transistors have been made [98] and verified experimentally [99], [100]. As for the MOS transistor, the G-R noise is attributed to the depletion region, and hence to the transistor channel, where charge fluctuation at the impurity or defect centers occurs [101]. The theoretical and experimental study presented in Ref. [101] conclude that the G-R noise is distinctly different from the flicker and thermal noise of the MOS transistor. Nevertheless, the G-R noise values at low frequency are low compared to the flicker noise and thus this noise source is omitted in further noise analysis of MOS transistor.

### B.2.6 Shot noise

Another noise mechanism, known as shot noise, was first described by Schottky in 1918 [102]. Shot noise is a fluctuation of electric current being the consequence of a fluctuation in the number of charges originating from a series of independent events occurring at random [82]. In other words, this noise is associated with direct current flow exhibiting the corpuscular nature of the electronic charges that cross a potential barrier. The electron “hop events” are independent and show the randomness of the arrival time. As an example, shot noise occurs in a *p-n* junction diode, where the passages of carriers (electrons and holes) across the potential barriers are independent of one another, so the individual current pulses carrying charge $q$ are random and not correlated. The spectral

distribution of shot noise is constant over all frequencies. and it depends only on the average current $I_{DC}$ and electronics charge $q$, as expressed in Eq. B.14 [82] :

$$S_{ish} = 2qI_{DC}. \tag{B.14}$$

In MOS transistors the shot noise is associated with the leakage current of drain-bulk and source-bulk inverse diodes as well as with the gate leakage current. However, these leakage currents are small and thus their effect can be neglected in most of practical circuits [95].

The most significant shot noise appears in reverse-biased diode employed as semiconductor detectors. Thus, the noise analysis of the readout electronics DC coupled to the semiconductor detectors has to include the shot noise related to the detector leakage current.

# Appendix C

# Modelling of noise in the front-end amplifiers

The theoretical analysis of the front end preamplifier presented in this thesis consists of the following steps:

1. Identification of all the noise sources that occur at the preamplifier input. The most important noise sources are related to the preamplifier input transistor, however the devices employed in the feedback loop and amplifier load have to be investigated as well. Each noise process, which is taken into account, has to be represented by an equivalent current or voltage generator and described by a given PSD.

2. Estimation of the preamplifier transfer function that describes how input signal is amplified and shaped by the preamplifier while being transfered to the output node.

3. Calculation of the total RMS noise value, that is seen at the preamplifier output node as an effect of superimposed noise sources identified above. This point is based on Eq. B.3.

4. Calculation of the ENC noise value expressed in electrons.

The noise analysis presented below has been performed for the preamplifier architecture employed in the AFRP chip, which is described in Chapter 3 (see Fig. 3.2). Similar noise analysis of the ABCN-25 preamplifier can be found in Ref. [64]. The AFRP preamplifier architecture provides two separate modes of operation: acquisition and reset, as explained in Chapter 3. A large number of parameters used in the noise calculations have to be determined separately for each mode of operation. In addition,

the signal transfer function provided by the preamplifier differs substantially for each operation mode. Therefore, the noise analysis of the circuit, which operates in the reset mode and then is switched to the acquisition mode for a given time period $t_{acq}$, is quite complex, and in principle, should be prformed in the time domain. In this work a method based on an approximation in the frequency domain has been employed. It combines the results of noise analysis performed separately for the reset and acquisition modes with a correction factor related to the effect of switching the preamplifier from the reset to the acquisition mode.

## C.1 Noise related to the preamplifier operating in the reset mode

During the reset phase, the preamplifier works as a transimpedance amplifier, where the feedback capacitor is discharged by an equivalent feedback resistance equal to $1/g_{m4}$. The $g_{m4}$ is the transconductance of feedback transistor M4 biased with reset current $I_{reset}$. Since the reset current directly drives the equivalent feedback resistance and so the preamplifier gain, the results of noise calculations for the reset phase are presented as a function of $I_{reset}$.

The analysis are carried in two following steps:

1. Contribution of the parallel and the series noise is estimated for the preamplifier working in the reset mode.

2. Propagation of reset phase noise to the preamplifier operating in the acquisition phase is estimated.

### C.1.1 Noise in the reset phase

In the reset phase the channel thermal noise of transistors M1, M3, M4 and M6, shown in Fig. 3.2 (see Section 3.3), is taken into account. It can be represented by a combination of parallel and series noise generators, as described below.

#### Parallel noise

The parallel noise generator $I_n$ shunting the preamplifier input is shown in Fig. C.1. It includes the channel thermal noise of two transistors: M4 and M6.

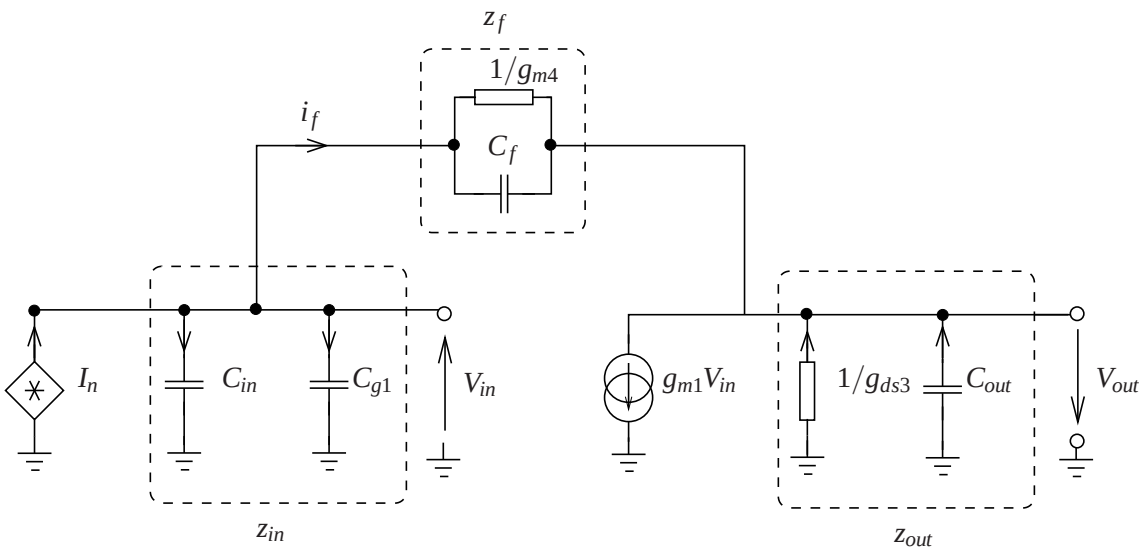



**Figure C.1:** Equivalent circuit of the preamplifier working in the reset mode. The parallel noise source is represented as current generator $I_n$ at the input node.

Using Eq. B.6 and Eq. B.7, the noise generated by transistors M4 and M6 can be described by the following PSDs:

$$S_{ithM4}(f) = 4kTn\gamma g_{m4}, \tag{C.1}$$

$$S_{ithM6}(f) = 4kTn\gamma g_{m6}, \tag{C.2}$$

The preamplifier transfer function $T_{i-r}(t)$, which describes the amplifier response $V_{out}(t)$ to the input current signal $I_n(t)$ is defined as:

$$T_{i-r}(t) = \frac{V_{out}(t)}{I_n(t)}. \tag{C.3}$$

In order to calculate the RMS value of output noise (see Eq. B.3), one has to integrate the noise spectrum shaped in the frequency domain by transfer function $T^2_{i-r}(f)$. According to the small signal model of the preamplifier, presented in Fig. C.1, one can write the following equations in the *s*-domain, in order to find the frequency transfer function $T_{i-r}(f)$:

$$\begin{cases} I_n = i_f + V_{in}/z_{in}) \\ i_f = g_{m1}V_{in} - V_{out}/z_{out}; \\ i_f z_f = V_{in} + V_{out} \end{cases} \tag{C.4}$$

where $i_f$ is the current flowing through the feedback loop,

$$z_{in} = \frac{1}{s(C_{in} + C_{g1})}, \tag{C.5}$$

$$z_f = \frac{1}{g_{m4} + sC_f}, \tag{C.6}$$

$$z_{out} = \frac{1}{g_{ds3} + sC_{out}}, \tag{C.7}$$

and

$$s = 2\pi i f. \tag{C.8}$$

By using equations C.4–C.8, the transfer function in the frequency domain can be written as:

$$T_{i-r}(f) = -\frac{(1 + g_{m1} z_f) z_{in} z_{out}}{z_f + z_{in} - z_{out} + g_{m1} z_{in} z_{out}}. \tag{C.9}$$

Then, employing the Eq. C.1, C.2 and C.9, the RMS value of noise originated from transistor M4, seen at the output of preamplifier, can be expressed by:

$$V_{rmsM4-r} = \sqrt{\int_0^\infty S_{ithM4}(f) |T_{i-r}(f)|^2 df}. \tag{C.10}$$

and for transistor M6 by:

$$V_{rmsM6-r} = \sqrt{\int_0^\infty S_{ithM6}(f) |T_{i-r}(f)|^2 df} \tag{C.11}$$

The final formulas for RMS noise values are quite complex, therefore the numerical values of parameters, as listed in Tab. C.1, have been used for calculating integrals C.10 and C.11. The results are plotted at the end of this section (Fig. C.3).

**Table C.1:** The numerical values of preamplifier parameters taken from simulations in SPICE.

| MOS transistor model parameters | | | |
|---|---|---|---|
| Symbol | Description | Value | Units |
| $C_{int}$ | total input capacitance including detector capacitance $C_{det}$, input transistor gate capacitance $C_{g1}$ modeled by employing Eq. A.10 and parasitic capacitance extracted from the layout | 40 | fF |
| $C_f$ | feedback capacitance | 1.3 | fF |
| $C_{out}$ | total output capacitance including physical output capacitance and parasitic capacitance extracted from the layout | 100 | fF |
| $g_{m1}$ | transconductance of transistor M1 | 40 | µS |
| $g_{m3}$ | transconductance of transistor M3 | 15 | µS |
| $g_{ds3res}$ | output conductance of transistor M3 while preamplifier operates in the reset phase | 28 | nS |
| $g_{ds3acq}$ | output conductance of transistor M3 while preamplifier operates in the acquisition phase | 6 | nS |
| $g_{ds3res}$ | output conductance of transistor M3 while preamplifier operates in the reset phase | 28 | nS |
| $\tau_b$ | integration time constant related to the buffer stage | 5 | ns |
| $W$ | gate width of transistor M1 | 6 | µm |
| $L$ | gate length of transistor M1 | 0.28 | µm |
| $W_{M3}$ | gate width of transistor M3 | 5.11 | µm |
| $L_{M3}$ | gate length of transistor M3 | 1.2 | µm |

### Series noise

The series noise is represented by an equivalent voltage noise generator $V_n$, as shown on Fig. C.2. The $V_n$ describes the thermal noise of cascode transistors M1 and M3. The PSDs of the series noise sources are represented by the following equations:

$$S_{vthM1} = \frac{S_{ithM1}}{g_{m1}^2}, \quad \text{where} \quad S_{ithM1} = 4kTn\gamma g_{m1}, \tag{C.12}$$

$$S_{vthM3} = \frac{S_{ithM3}}{g_{m1}^2}, \quad \text{where} \quad S_{ithM3} = 4kTn\gamma g_{m3}, \tag{C.13}$$

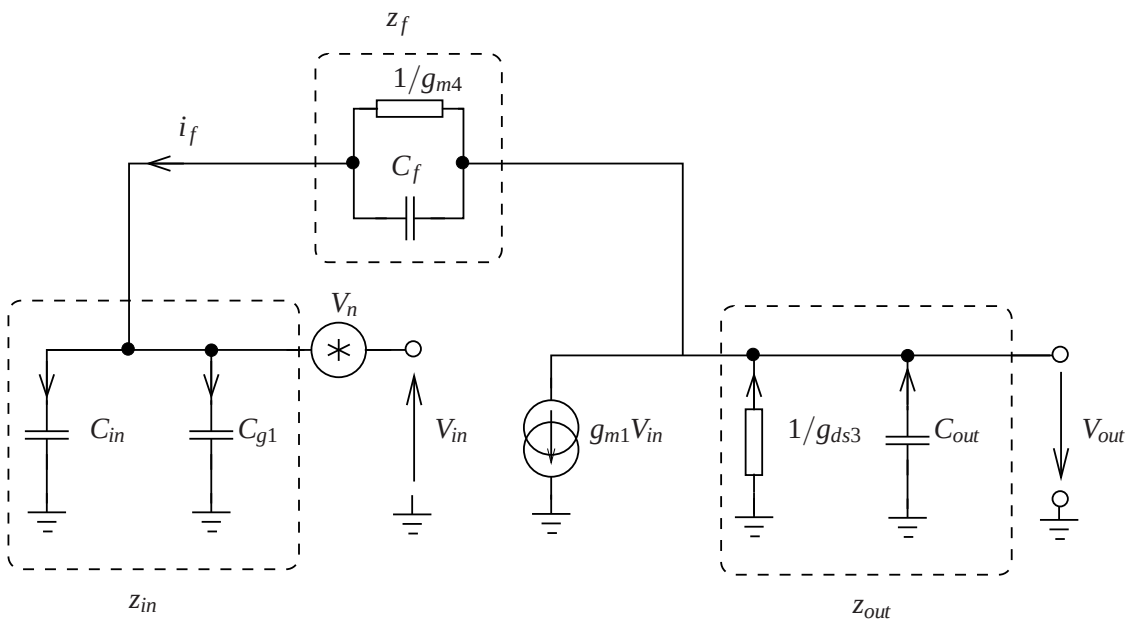



**Figure C.2:** Equivalent circuit of the preamplifier working in the reset mode. The series noise source is represented as voltage generator $V_n$ connected to the preamplifier input node.

The transfer function of the series noise $T_{v-r}(t)$ is defined by $V_{out}/V_n(t)$ factor and can be calculated based on following equations:

$$\begin{cases} \frac{V_{out}}{z_{out}} = g_{m1}V_{in} + i_f, \\ V_{in} - V_n + i_f z_f = 0, \\ \frac{V_{in}-V_n}{z_{in}} = -\frac{V_{out}}{z_{in}+z_f}. \end{cases} \tag{C.14}$$

Employing equations C.5–C.8 and C.14 the transfer function in the frequency domain $T_{v-r}(f)$ is given by:

$$T_{v-r}(f) = \frac{(z_{in}+z_f)z_{out}g_{m1}}{z_{in}z_{out}g_{m1} + z_{out} + z_{in} + z_f}. \tag{C.15}$$

Finally, the RMS noise values at the preamplifier output, originating from transistors M1 and M3, can be calculated as follows:

$$V_{rmsM1-r} = \sqrt{\int_0^\infty S_{vthM1}|T_{v-r}(f)|^2 df}, \tag{C.16}$$

$$V_{rmsM3-r} = \sqrt{\int_0^\infty S_{vthM3}|T_{v-r}(f)|^2 df}, \tag{C.17}$$

Similarly as for the parallel noise, the numerical values of parameters, as listed in Tab. C.1, have been applied in calculation of integrals C.16 and C.17. The comparison of RMS output noise originating from transistors M1, M3, M4 and M6 is shown in Fig. C.3.

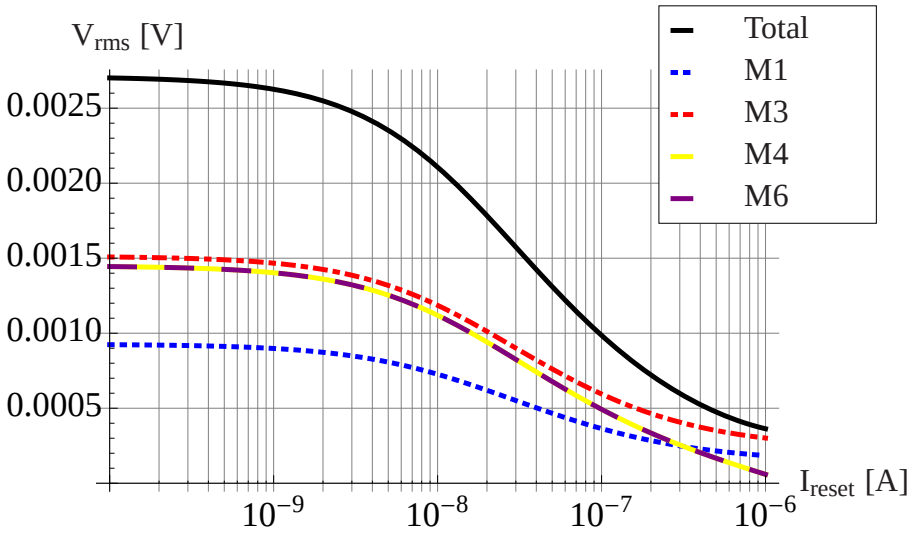



**Figure C.3:** Calculated reset phase noise.

## C.1.2 Propagation of the reset noise to the acquisition phase

The reset phase noise itself is not the key value, but it is important to estimate how this noise influences the circuit operating in the acquisition phase. It is assumed that the output noise signal originated from the reset phase while switching the circuit from the reset to the acquisition phase is fed back to the preamplifier input node and sampled there. This approach introduces an additional input noise component, which has to be taken into account in the acquisition phase noise analysis. This noise component is then amplified and shaped with the acquisition phase transfer function. In order to calculate this effect the additional factor $K$ is introduced. This factor describes how the reset phase voltage noise is seen at the preamplifier output during the acquisition phase. According to schema presented in Fig. C.4 the following equation can be written

$$V_{in} g_{m1} = \frac{(V_{out} - V_{in})}{z_f} + \frac{V_{out}}{z_{out}}. \tag{C.18}$$

where $z_{out}$ is defined by Eq. C.7. The transfer function, defined as $V_{out}/V_{in}$ ratio, is calculated based on Eq. C.18 as follows:

$$T_v(s) = \frac{(1+g_{m1}z_f)z_{out}}{z_f + z_{out}} \tag{C.19}$$

where $z_{out}$ is defined by C.7, and $z_f$ can be expressed as follows:

$$z_f = \begin{cases} \frac{1}{g_{m4}+sC_f} & \text{for reset phase} \\ \frac{1}{sC_f} & \text{for acquisition phase} \end{cases} \tag{C.20}$$

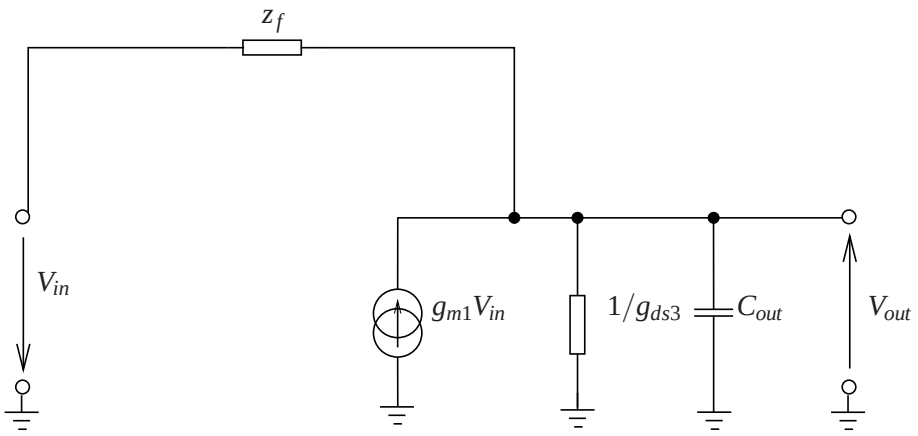



**Figure C.4:** Small signal model of the circuit useful for calculating input-to-output voltage transfer function.

Finally, the $K$ factor, which describes propagation of the calculated reset phase noise, presented in Fig. C.3, to the acquisition phase is defined as the division of transfer functions in the acquisition phase $T_{v-a}$ by the one in the reset phase $T_{v-r}$:

$$K = \frac{T_{v-a}}{T_{v-r}}, \tag{C.21}$$

The $T_{v-a}$ and $T_{v-r}$ in Eq. C.21 are defined by Eq. C.19 with different $z_f$ values, as described by Eq. C.20. Employing the $K$ factor, the RMS voltage noise of the transistors M1, M3, M4 and M6, seen at the output of preamplifier during acquisition phase, are given by:

1. Parallel noise representing channel thermal noise of transistors M4 and M6:

$$V_{rmsM4-a} = \sqrt{\int_0^\infty S_{ithM4}(f)|T_{i-r}(f)|^2|K(f)|^2 df}, \tag{C.22}$$

$$V_{rmsM6-a} = \sqrt{\int_0^\infty S_{ithM6}(f)|T_{i-r}(f)|^2|K(f)|^2 df}. \tag{C.23}$$

2. Series noise representing channel thermal noise of transistors M1 and M3:

$$V_{rmsM1-a} = \sqrt{\int_0^\infty S_{vthM1}|T_{v-r}(f)|^2|K(f)|^2 df}, \tag{C.24}$$

$$V_{rmsM3-a} = \sqrt{\int_0^\infty S_{vthM3}|T_{v-r}(f)|^2|K(f)|^2 df}, \tag{C.25}$$

The calculation results are presented in Fig. C.5.

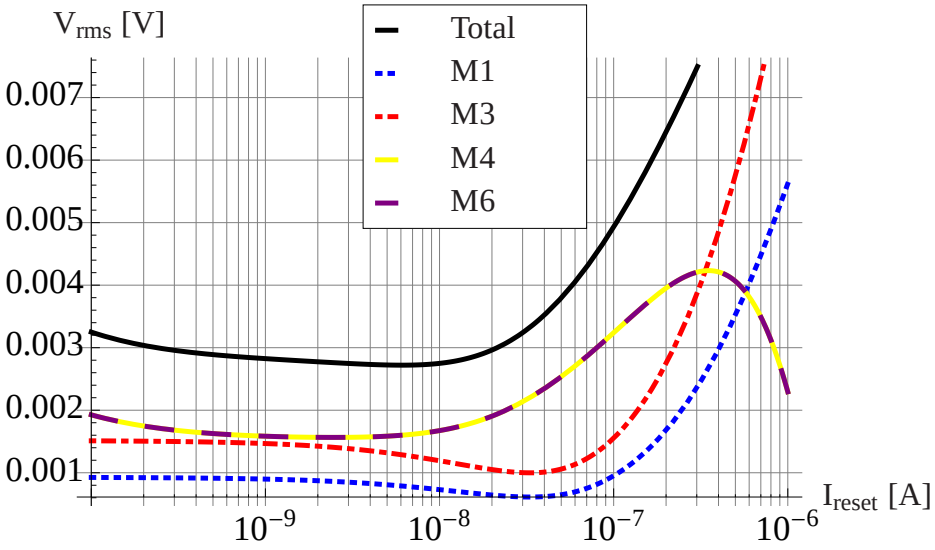



**Figure C.5:** Propagation of the reset noise to the acquisition phase.

In order to compare the reset phase noise propagated to the acquisition phase with the noise originating in the acquisition phase, the calculated terms shown in Fig. C.5 should be expressed as ENC, what can be calculated as follows:

$$ENC = \frac{V_{rms}}{G \cdot q}, \tag{C.26}$$

where G is a charge gain of the preamplifier in the acquisition phase, defined by Eq.C.27

$$G = \frac{1}{C_f}. \tag{C.27}$$

## C.2 Noise related to the preamplifier operating in the acquisition mode

On top of the noise related to the reset phase the following noise sources are present in the preamplifier operating in the acquisition phase:

- noise related to transistor M1 — $S_{iTH1}$, $S_{iGIC1}$ and $S_{iF1}$ depicted in Fig. C.6,
- noise related to transistor M3 — $S_{iTH1}$ shown in Fig. C.6,
- shot noise from the detector leakage current — $S_{ish}$ presented in Fig. C.6.

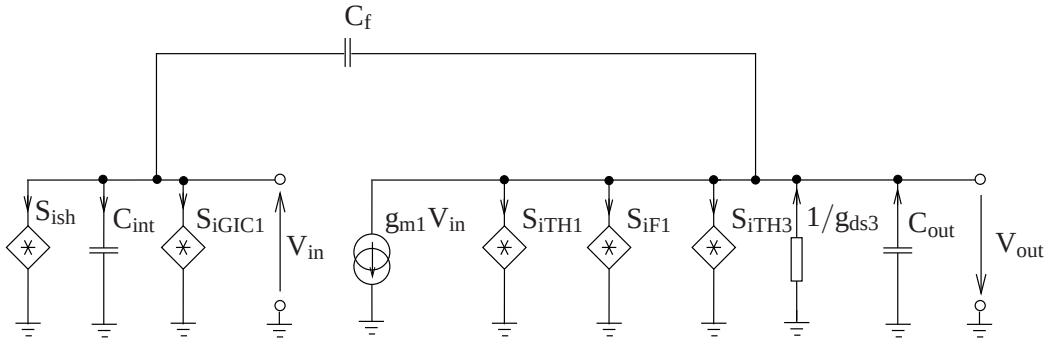



**Figure C.6:** Noise sources originating from the preamplifier operating in the acquisition phase.

These noise sources can be described as combination of a current noise signal generator shunting the preamplifier input and a series voltage noise signal generator (see Figs. C.1 and C.2). The preamplifier operating in the acquisition mode contains capacitor in the feedback loop and no equivalent feedback resistance. Thus, the feedback impedance $z_f$ describe by Eq. C.6 has to be redefined following Eq. C.20 for the acquisition phase:

$$z_f = \frac{1}{sC_f}. \tag{C.28}$$

This feedback impedance $z_f$ (Eq. C.28) is applied to the preamplifier transfer functions C.9 (for the parallel noise) and C.15 (for the series noise) in order to recalculate these terms, obtaining in the acquisition phase transfer functions $T_{i-a}(f)$ and $T_{v-a}(f)$ for the parallel and series noise respectively:

$$T_{i-a}(f) = \frac{(g_{m1} - 2iC_f\pi f)}{2i\pi f(C_{int}(g_{ds3acq} + C_{out}2i\pi f) + C_f(g_{ds3acq} + g_{m1} + (C_{int} + C_{out})2i\pi f))}, \tag{C.29}$$

$$T_{v-a}(f) = \frac{g_{m1}(C_f + C_{int})}{C_{int}(g_{ds3acq} + C_{out}2i\pi f) + C_f(g_{ds3acq} + g_{m1} + (C_{int} + C_{out})2i\pi f)}. \quad \text{(C.30)}$$

These transfer functions, $T_{i-a}(f)$ and $T_{v-a}(f)$, introduce the effect of limited bandwidth of the non-buffered cascode stage on the overall noise spectrum. In addition, one should keep in mind that a finite measurement time $t_{acq}$ cuts off the low frequency noise components for f$\leq 1/t_{acq}$. Thus, it is assumed that the overall shaping function of the preamplifier is equivalent to a gated integrator, where the integration time constant is defined by the bandwidth of the unbuffered cascode stage loaded with the input, output and feedback capacitances, whereas the measurement time $t_{acq}$ attenuates the noise spectra at low frequency.

The approximation of the transfer function is based on introducing the signal attenuation factor at the low frequencies, where the signal period is much longer than the acquisition time $t_{acq}$. It is also required that this transfer function does not change the amplitude of the signals for the frequencies above $1/t_{acq}$ and it should give simple solution for the definitive integrals for the ENC calculation. Finally, the transfer function of a high pass filter was employed, as described by Eq. C.31

$$T_{gate}(f) = \frac{2ft_{acq}}{\sqrt{1 + (2ft_{acq})^2}}. \quad \text{(C.31)}$$

### C.2.1 Parallel noise

The parallel current generator $I_n$ in Fig. C.1 includes the following noise sources valid in the acquisition mode:

1. Gate induced current noise of transistor M1. The PSD defined by Eq. B.12 has been found as follows:

$$S_{iGICM1} = \frac{32C_{OXU}^2 kL^2 TW^2 \gamma (2\pi f)^2}{45 g_{m1} n}, \quad \text{(C.32)}$$

   where $C_{OXU}$ is the unitary gate oxide capacitance, $W$ and $L$ are the width and length of the input transistor M1, and $f$ is frequency.

2. Shot noise originated from the detector leakage current $I_{leak}$. The PSD defined by Eq. B.14 can be described as follows:

$$S_{ish} = 2qI_{leak}. \quad \text{(C.33)}$$

The expressions for the PSDs and the transfer functions $T_{i-a}(f)$ (Eq. C.29) and $T_{gate}(f)$ (Eq. C.31) are used for calculation of RMS output noise as follows:

1. GIC noise:

$$V_{rms\_M1GIC} = \sqrt{\int_0^\infty S_{iGICM1}|T_{i-a}(f)|^2|T_{buff}(f)|^2|T_{gate}(f)|^2 df}. \tag{C.34}$$

   In this equation an additional factor $T_{buff}(f)$ has been introduced, which is a low-pass filter transfer function $1/(1+2\pi f\tau_b)$, where $\tau_b$ is an integration time constant related to the buffer stage used in the row and column readout of the pixel matrix. According to circuit simulations carried in SPICE $\tau_b$ equals 5 ns.

2. Shot noise from detector leakage current:

$$V_{rms\_sh} = \sqrt{\int_0^\infty S_{ish}|T_{i-a}(f)|^2|T_{gate}(f)|^2 df}. \tag{C.35}$$

### C.2.2 Series noise

The series voltage generator $V_n$ in Fig. C.2 represents the following noise sources:

1. Channel thermal noise of the input transistor M1. The PSD is defined by Eq. C.12.
2. Channel thermal noise of the cascode load transistor M3. The PSD is defined by Eq. C.13.
3. Flicker noise with PSD defined by Eq. B.10 where the flicker noise coefficient $K_a$ can be found in Tab. A.1.

These expressions for PSDs and the transfer functions $T_{v-a}(f)$ (Eq. C.30) and $T_{gate}(f)$ (Eq. C.31) are employed for calculation of RMS output noise as follows:

1. Channel thermal noise of the input transistor M1:

$$V_{rms\_M1TH} = \sqrt{\int_0^\infty S_{vthM1}|T_{v-a}(f)|^2|T_{gate}(f)|^2 df}. \tag{C.36}$$

2. Channel thermal noise of the cascode load transistor M3:

$$V_{rms\_M3TH} = \sqrt{\int_0^\infty S_{vthM3}|T_{v-a}(f)|^2|T_{gate}(f)|^2 df}. \tag{C.37}$$

3. Flicker noise:

$$V_{rms\_M1F} = \sqrt{\int_0^\infty S_{vFM1}|T_{v-a}(f)|^2|T_{gate}(f)|^2 df}. \tag{C.38}$$

Furthermore, since the calculations are carried out in the frequency domain, the term related to the correlation between the channel thermal noise and the GIC noise has to be included. The RMS noise value of this correlation term has been found as follows:

$$V_{rms\_corr} = \sqrt{\int_0^\infty V_{corr}^2|T_{gate}(f)|^2 df}. \tag{C.39}$$

where $V_{corr}$ has been calculated following the noise analysis described in Ref. [64]:

$$V_{corr} = 2Im\left[S_{iF1}\right] T_{i-a}(f) \left[T_{v-a}(f)\right]^* \frac{1}{g_{m1}}. \tag{C.40}$$

The $S_{iF1}$ in Eq. C.40 is defied by Eq. B.13.

The ENC terms corresponding to RMS noise expressions listed above, are calculated by using the Eq. C.26. Final ENC expressions are shown in Section 3.4.1 of Chapter 3.

# Table of acronyms

| | |
|---|---|
| ABCN-25 | ATLAS Binary Chip Next |
| AC | Alternate-Current |
| AFRP | Amorphous Frame Readout Pixel |
| ALICE | A Large Ion Collider Experiment |
| ATLAS | A Toroidal LHC ApparatuS |
| CCD | Charged Coupled Devices |
| CERN | European Organization for Nuclear Research |
| CLIC | Compact LInear Collider |
| CMOS | Complementary Metal Oxide Semiconductor transistor |
| CMS | Compact Muon Solenoid |
| DAC | Digital-to-Analog Converter |
| DC | Direct-Current |
| DCR | Detector Concept Report |
| DEPFET | DEPleted Field Effect Transistor structure |
| DMILL | Durcie Mixte sur Isolant Logico-Lineaire |
| DNL | Differential NonLinearity |
| EKV | the Enz-Krummenacher-Vittoz model |
| ENC | Equivalent Noise Charge |
| FE | Front-End |
| FET | Field Effect Transistor |
| GDE | Global Design Effort |
| HEP | High Energy Physics |
| HERA | Hadron Elektron Ring Anlage |
| HPS | Hybrid Pixel Sensor |
| IBM | International Business Machines |
| ID | Inner Detector |
| ILC | International Linear Collider |
| ILD | International Large Detector |
| IR | interaction region |
| INL | Integral Nonlinearity |

| | |
|---|---|
| LEP | Large Electron Positron Collider |
| LHC | Large Hadron Collider |
| LHCb | Large Hadron Collider beauty |
| LSB | Least Significant Bit |
| MAPS | Monolithic Active Pixel Sensor |
| MIP | Minimum Ionizing Particle |
| MOS | Metal-Oxide Semiconductor transistor |
| MOSFET | Metal-Oxide Semiconductor Field-Effect Transistor |
| NMOS | N-type Metal-Oxide-Semiconductor transistor |
| PETS | Power Extraction and Transfer Structures |
| PMOS | P-type Metal-Oxide-Semiconductor transistor |
| PVT | Process-Voltage-Temperature |
| RMS | Root Mean Square |
| RF | Radio Frequency |
| SCT | SemiConductor Tracker |
| SEU | Single Event Upset |
| SiD | Silicon Detector |
| S-LHC | Super LHC |
| SM | Standard Model |
| SMD | Surface Mount Device |
| SNR | Signal-to-Noise Ratio |
| SOI | Silicon-On-Insulator |
| SPL | Superconducting Proton Linac |
| SSD | Silicon Strip Detector |
| SSDT | Silicon Strip Detector Tracker |
| TBA | Two-Beam Acceleration |
| TFA | Thin Film on ASIC |
| TRT | Transition Radiation Tracker |

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# Acknowledgements

First and foremost, I offer my sincerest gratitude to my supervisor Prof. Władysław Dąbrowski from AGH University of Science and Technology in Cracow, for his support in the Ph.D. program. He has been always there to help, to give advice and to explain things clearly and simply. Throughout my thesis-writing period, he provided encouragement, valuable advice and constructive comments on this thesis. Without his knowledge, assistance and patience, this study would not have been successful.

A special thanks goes to the supervisor of my fellowship at CERN, Dr. Jan Kapłon from the Electronics Systems for Experiments Group (PH-ESE). He has taught me the art of analog integrated circuits design and he introduced me to theoretical noise calculations. His constant support has been invaluable at each stage of my work. His PhD thesis was a great guide throughout my work on low-noise preamplifiers. I am grateful for his encouragement, effort, guidance and all the table tennis matches we had after work to refresh our minds. Without Jan, my work on this thesis would have been much more difficult.

I am heartily thankful to Prof. Danuta Kisielewska for her encouragement to continue my research carrier after my Masters; I am glad I followed her advice.

I would like thank Dr. Pierre Jarron for insightful discussions on the AFRP chip.

I would like to thank Prof. Christophe Ballif, Dr. Matthieu Despeisse and Dr. Nicolas Wyrsch from Institute of Microengineering at Ecole Polytechnique Fédérale de Lausanne for preparing the sensor deposition on AFRP chip and for valuable technical discussions on the TFA technology.

I thank Dr. Rafael Ballabriga, who has provided me with good hints for the design of DACs.

Many thanks to Dr. Giovanni Anelli for an access to his DAC design library.

I am grateful to Michał Dwużnik for his time spent on characterisation and irradiation tests of the ABCN-25 chip.

Special thanks to Bert Van Koningsveled and Wojtek Bialas for constant support with the computers, software and in particular, the Cadence tools.

Many thanks to Dr. Alessandro Marchioro, the leader of the Micro Electronics section of PH-ESE and Dr. Paulo Moreira for their support and patience during period in which I wrote this thesis.

I am grateful to all my friends and colleagues from PH-ESE Group at CERN for the pleasant working atmosphere they have created.

I thank Dr. Grzegorz Deptuch from Fermilab for his friendship and great enthusiasm on analog integrated circuits design.

I also warmly thank Ryan, Piotr, Julia, Michał and Michał for time they have spent reading my thesis.

I am grateful to my beloved people in Poland: Konrad, Ania, Sewi, Ala, Iwonka, Sebastian, Krzyś, Tomek and Krzysztof for their support and friendship.

My warmest gratitude goes also to a great people I have met during my stay in Geneva: to all my Polish friends (far too many people to mention individually), to Winnie, Fatima, Maria, Jenni, Mamad, Antonio, Alex and Ernesto.

Many thanks to musicians from Miss Proper and the Moving Targets. They have given me so much energy during the preparation of this thesis.

Finally, I am forever indebted to my parents, Maria and Kazimierz, and to my grandparents, Teresa and Józef, for their love, understanding, patience, endless support, never-failing faith in me and for great Polish food that was always waiting for me at home.